30mA 2-channel LDO voltage regulator (output voltage each channel 1.0V)

OVERVIEW

028SAM_LDO_04 is external-capacitor-based Linear Regulator in Samsung 28 FD-SOI to generate SoC voltage supply voltage. It contains two independently programmable drivers to generate stable voltage in the range of 0.9V to 1.1V.

LDO is intended to maintain load current 30mA – 50mA.

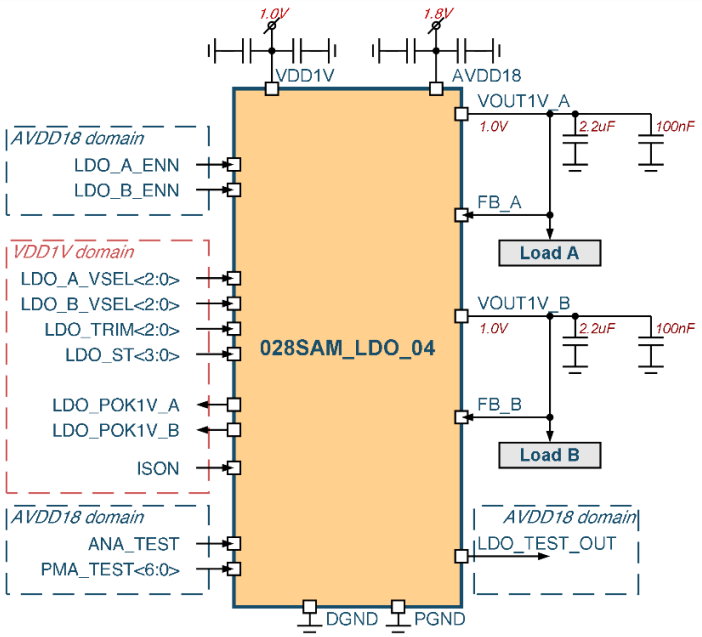
The 028SAM_LDO_04 embeds a voltage reference 0.6V, voltage-to-current converter for biasing and logic control.

A Power-OK signals notify the system has completed its booting sequence and if its output is maintaining regulation for the current drawn by the load.

IP technology: Samsung 28nm FDSOI technology process.

IP status: silicon proven.

Area: 0.12mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Operating junction temperature	T_J	-		-40	27	125	°C
Analog supply voltage	AVDD18	-		1.62	1.8	1.98	V
Digital supply voltage	VDD1V	-		0.95	1.00	1.05	V
Output current	I_{OUT}	For each output VOUT1V_A and VOUT1V_B		0.1	30	50	mA
External output capacitor	C_{OUT1}	for each output VOUT1V_A and VOUT1V_B	ESR = 30mΩ	-	2.2	4.7	µF
	C_{OUT2}		-	-	100	-	nF
Quiescent current	I_{Q_AVDD18}	I_{OUT} = 30mA for each output VOUT1V_A and VOUT1V_B, AVDD18 = 1.8V	Full operation mode	80	120	225	µA
			Single output mode	45	65	110	µA
			BGV+V2I only	5	7	9	µA
	I_{Q_VDD1V}	VDD1V = 1.0V	Full operation mode	-	0.5	10	nA
Shutdown current	I_{SD_AVDD18}	LDO_ENN= AVDD18, @GND	Full operation mode	4	5	61	µA
	I_{SD_VDD1V}			1	3	56	nA
Regulated output voltage	V_{OUT1V}	For each output VOUT1V_A and VOUT1V_B		0.94	1.0	1.04	V
DC accuracy	A_{OUT}	with BGV+V2I		-7.7	-	6.5	%
Load transient response	ΔV_{OUT}	I_{OUT} = 10mA –> 30mA (undershoot)T_j = 27°C		-	3.2	3.7	%
Power supply rejection ratio	PSRR	T_j=-40°C÷+125°C, AVDD18=1.62V÷1.98V, I_{OUT}=30 mA, Cload =2.2 uF and 100nF	f = 400kHz	-	-73	-43	dB
			f = 1MHz	-	-69	-51	
			f = 12MHz	-	-75	-65	
Voltage reference value	VREF	Over PVT		565	600	618	V
Voltage reference value accuracy	A_{VREF}	without trimming		-5.7	-	4.8	%
Voltage reference load capability	I_{LOAD_BG}	-		-	-	15	nA
POK threshold voltage (asserted)	TH_{POK_R}	for each output VOUT1V_A and VOUT1V_B		0.81	0.86	0.89	V