# 1mA LDO voltage regulator (output voltage 0.4V…0.9V)

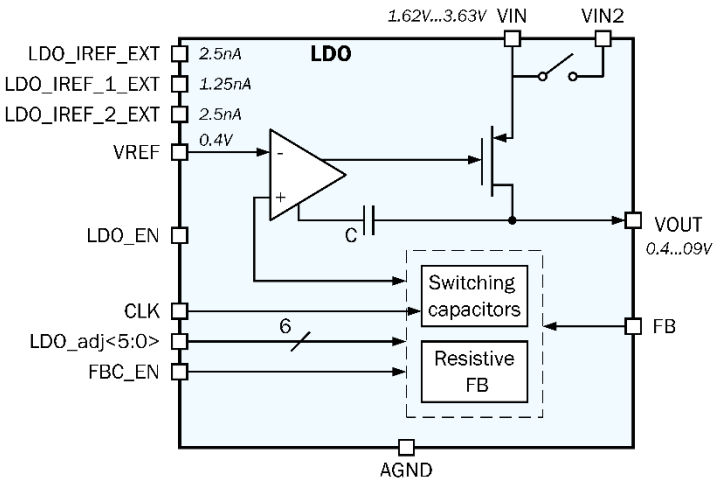
## OVERVIEW

040TSMC_LDO_01 is a low drop out voltage regulator designed to supply integrated circuits with stable and precise voltage. The LDO receives the input voltage VIN +1.62V…+3.63V and converts this voltage into a voltage VOUT 0.4V…0.9V. This voltage is programmed by the MCU using the bus LDO_adj <5:0> and adjustable from 0.4V to 0.9V. The block consists of a differential amplifier, pass transistor, resistive and capacitive divider.

IP technology: TSMC 40nm CMOS ULP technology

IP status: silicon proven

Total area: 0.04mm$^2$




## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | min | typ. | max | |
| Input voltage | $V_{IN}$ | - | 1.62 | - | 3.63 | V |
| Output voltage | $V_{OUT}$ | - | 0.4 | - | 0.9 | |
| Operating junction temperature | $T_j$ | - | -40 | +27 | +100 | °C |
| External reference current | $I_{REF\_EXT}$ | Fclk = 2kHz | 2.25 | 2.5 | 2.75 | nA |
| | | | 1.125 | 1.25 | 1.375 | |
| | | | 2.25 | 2.5 | 2.75 | |
| | | Fclk=16kHz | 7.6 | 21.3 | 24.6 | nA |
| | | | 3.7 | 10.5 | 12 | |
| | | | 7.6 | 21.3 | 24.6 | |
| Reference voltage | $V_{ref}$ | - | 0.4 - 4% | 0.4 | 0.4 + 4% | V |
| Bus output voltage control resolution | - | - | - | 6 | - | bit |
| LSB step UP setting time | - | Vin=1.62V, Fclk=2kHz, LDO_adj<5:0>=0.9V, Cload=5uF, Iload=100nA, FBCen=1 | - | 2.7 | 3.7 | ms |
| Quiescent current consumption (the reference current value included) | Iq | Fclk=2kHz, Iload=100nA, LDO adj<5:0>=0.9V, FBCen=1, Cload=2uF | - | 17.5 | 20 | nA |
| | | Fclk=16kHz, Iload=1mA, LDO adj<5:0>=0.9V, FBCen=1,Cload=2uF | - | 280 | 325 | nA |
| | | Fclk=16kHz, Iload= 1mA, LDO_adj<5:0>=0.9V, FBCen=0, Cload=5uF, During start | - | 701 | 860 | nA |
| Start up time | t | Fclk=16kHz, LDO_adj<5:0>=0.9V, FBCen=0, Cload=5uF | - | 5 | 9.6 | ms |
| Leakage current when disabled | Il | Input signals are Vin or ground. ldo_enable=0 | - | 0.04 | 0.83 | nA |
| Maximum load current | $I_{load\ max}$ | - | - | - | 1 | mA |
| External clock frequency | $F_{clk}$ | - | - | 2 | 16 | kHz |
| Input logic-level low | $V_{IH}$ | - | - | - | 0.2* $V_{IN}$ | V |
| Input logic-level high | $V_{IL}$ | - | 0.8* $V_{IN}$ | - | - | V |