5mA LDO voltage regulator (output voltage 1.1V/1.2V/1.3V/1.4V)

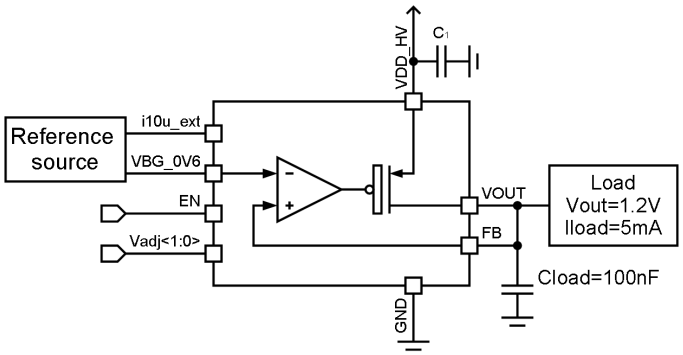
OVERVIEW

055TSMC_LDO_01 is a low drop out voltage regulator designed to supply integrated circuits with stable and precise voltage. The LDO inputs voltage VDD_HV 2.25… 3.6V and converts this voltage into a voltage VOUT 1.1V/1.2V/1.3V/1.4V with 5mA load capacity. This voltage programmed using the bus Vadj<1:0>.

IP technology: TSMC EF CMOS 55nm.

IP status: silicon proven.

Silicon area: 0.0154mm^2



ELECTRICAL CHARACTERISTICSДА

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V_{DD_HV}	-	2.25	-	3.6	V
Ambient temperature	T_j	-	-40	+25	+85	°C
Input logic-level high	V_{IH}	For digital inputs	V_{DD_HV}-0.25	-	V_{DD_HV}	V
Input logic-level low	V_{IL}		0	-	0.25	V
Current consumption	I_{VDD_HV}	I_{load} = 5mA	6.97	7.39	7.84	µA
		Power off	0.49	0.94	6.9	nA
Reference voltage	V_{VBG}	-	-	600	-	mV
Reference current	I_{ref}	-	-	10	-	µA
Maximum load current	I_{load}	-	-	-	5	mA
Output voltage	V_{OUT}	V_{adj}="00"; 1mA<I_{load}<5mA; 2.25V<V_{DD_HV}<3.6V	1.10	1.10	1.09	V
		V_{adj} ="01"; 1mA<I_{load}<5mA; 2.25V<V_{DD_HV}<3.6V	1.20	1.20	1.21	
		V_{adj} ="10"; 1mA<I_{load}<5mA; 2.25V<V_{DD_HV}<3.6V	1.30	1.30	1.31	
		V_{adj} ="11"; 1mA<I_{load}<5mA; 2.25V<V_{DD_HV}<3.6V	1.40	1.40	1.42	
Output voltage drop	V_{drop}	V_{DD_HV} = 3.3V; I_{load} = 5mA	58.2	88.8	136.4	mV
Output voltage deviation (in the load range)	δV_{load}	2.25<V_{DD_HV}<3.6V; I_{load}=5mA	-	-	1	%
Output voltage deviation (in supply voltage range)	δV_{VDD}	V_{DD_HV}=3.3V; 100uA< I_{load} <5mA	-	-	2.5	%
External load capacity	C_{load}	-	47	100	330	nF