

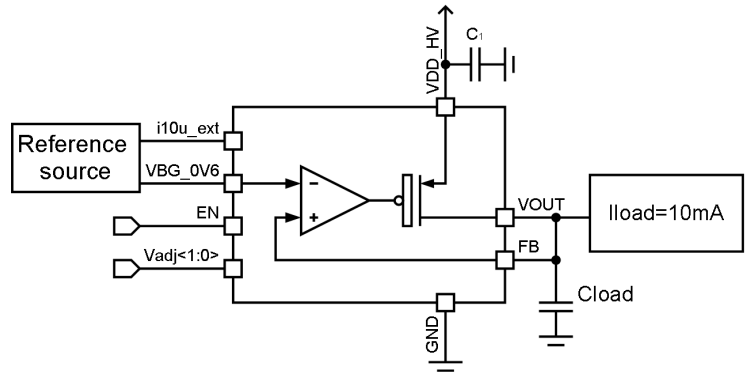
10 mA LDO voltage regulator (output voltage 1.1V/1.2V/1.3V/1.4V)
OVERVIEW

055TSMC_LDO_02 is a low drop out voltage regulator designed to supply integrated circuits with stable and precise voltage. The LDO inputs voltage V_{DD_HV} 2.25... 3.6V and converts this voltage into a voltage V_{OUT} 1.1V/1.2V/1.3V/1.4V with 10mA load capacity. This voltage programmed using the bus $V_{adj}<1:0>$.

IP technology: TSMC CMOS 55nm.

IP status: silicon proven.

Silicon area: 0.016mm²


ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V_{DD_HV}	-	2.25	-	3.6	V
Ambient temperature	T_j	-	-40	+25	+85	°C
Input logic-level high	V_{IH}	For digital inputs	$V_{DD_HV}-0.25$	-	V_{DD_HV}	V
Input logic-level low	V_{IL}		0	-	0.25	V
Current consumption	I_{VDD_HV}	$I_{load} = 10mA$	6.97	7.39	7.84	µA
		Power off	73.5	134	286.1	nA
Reference voltage	V_{VBG}	-	-	600	-	mV
Reference current	I_{ref}	-	-	10	-	µA
Maximum load current	I_{load}	-	-	-	10	mA
Output voltage	V_{OUT}	$V_{adj}="00"; 1mA < I_{load} < 10mA;$ $2.25V < V_{DD_HV} < 3.6V$	1.101	1.104	1.113	V
		$V_{adj}="01"; 1mA < I_{load} < 10mA;$ $2.25V < V_{DD_HV} < 3.6V$	1.200	1.202	1.206	
		$V_{adj}="10"; 1mA < I_{load} < 10mA;$ $2.25V < V_{DD_HV} < 3.6V$	1.301	1.302	1.309	
		$V_{adj}="11"; 1mA < I_{load} < 10mA;$ $2.25V < V_{DD_HV} < 3.6V$	1.400	1.401	1.404	
Output voltage accuracy	ΔV_{OUT}	$I_{load} = 1mA; T = 25^{\circ}C$	-0.75	-	+0.75	%
		$1mA < I_{load} < 10mA;$ $(V_{OUT} + 0.5V) < V_{DD_HV} < 3.6V$	-1.25	-	1.25	
Output voltage drop	V_{drop}	$V_{DD_HV} = 3.3V; I_{load} = 10mA$	92	145	217	mV
Output voltage deviation (in the load range)	δV_{load}	$2.25 < V_{DD_HV} < 3.6V;$ $I_{load} = 10mA$	-	-	1	%
Output voltage deviation (in supply voltage range)	δV_{VDD}	$V_{DD_HV} = 3.3V;$ $100\mu A < I_{load} < 10mA$	-	-	2.5	%
External load capacity	C_{load}	-	100	330	1000	nF