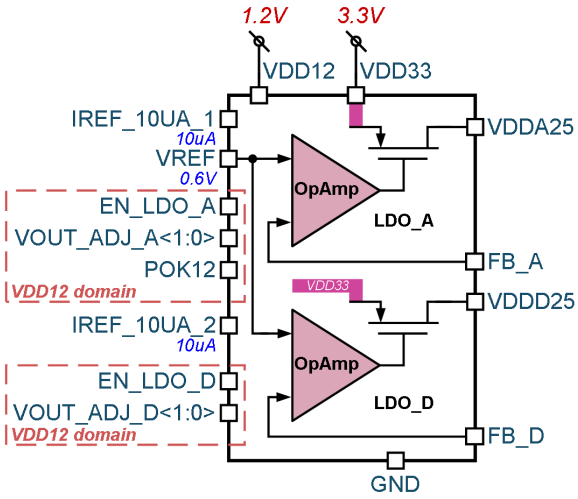
20mA and 500mA LDO voltage regulators (output voltage 2.5V)

OVERVIEW

055TSMC_LDO_06 is a cap-based LDO voltage regulator designed to supply integrated circuits with stable and precise voltage. 2.5V. The LDO converts IO voltage 3.3V to **VDDA25** (2.5V) to supply analog circuits with load up to 500mA and converts IO voltage 3.3V to **VDDD25** (2.5V) to supply digital circuits with load up to 20mA. Each output voltage can be programmable to required value. The block operates directly from two main power supplies: IO voltage **VDD33** and core voltage **VDD12** supply. The block requires external reference currents: **IREF_10UA_1** (10uA), **IREF_10UA_2** (10uA) and reference voltage **VREF** (0.6V).



IP technology: TSMC 55nm MS RF.
IP status: pre-silicon verification.
GDS area: 0.21mm^2.
Silicon area: 0.17mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
IO supply voltage	V_{DD33}	-		3.0	3.3	3.6	V
Core supply voltage	V_{DD12}	-		1.14	1.2	1.26	V
Operating temperature range	T_j	-		-40	+27	+85	°C
Load current	I_{LOAD_A}	-		-	500	-	mA
	I_{LOAD_D}	-		-	20	-	mA
Capacitive load	C_{LOAD_A}	-		-	22	-	uF
	C_{LOAD_D}	-		-	2.2	-	uF
Startup time	t_{ST}	EN_LDO_A and EN_LDO_D enabled		-	100	-	us
Input reference voltage	V_{REF}	-		-	0.6	-	V
Reference voltage accuracy	ΔV_{REF}	-		-	3	-	%
Input reference current	I_{10u}	-		-	10	-	uA
Reference current accuracy	ΔI_{REF_10u}	-		-	5	-	%
Output voltage	V_{DDA25}	@VDDA25		2.42	2.51	2.61	V
	V_{DDD25}	@VDDD25		2.42	2.51	2.60	V
Output voltage accuracy	ΔV_{DDA25}	@VDDA25		-	3.5	-	%
	ΔV_{DDD25}	@VDDD25		-	3.5	-	%
Current consumption in operating mode	I_{DD33}	T_j=-40÷85°C, I_{LOAD_D}=20mA, I_{LOAD_A}=500mA, V_{DD33}=3.3V, V_{DD12}=1.2V		37.87	40.02	41.72	uA
	I_{DD12}			0.12	3.50	9.51	nA
Current consumption in standby mode	I_{STB_DD33}			20.88	99.07	597.4	nA
	I_{STB_DD12}			0.13	3.4	9.27	
Line regulation	$\Delta V_{LINE}/\Delta V_{IN}$	@V_{DDA25}, T_j=25°C, I_{LOAD_A}=500mA		-	0.61	-	%/V
		@V_{DDD25}, T_j=25°C, I_{LOAD_D}=20mA		-	0.82	-	%/V
Power Supply Rejection Ratio	$PSRR_{VDDA25}$	T_j=-40°C÷+85°C, I_{LOAD_A} = 500mA	@10kHz	11	-	-	dB
			@100kHz	21	-	-	
			@1MHz	30	-	-	
	$PSRR_{VDDD25}$	T_j=-40°C÷+85°C, I_{LOAD_D} = 20mA	@10kHz	9	-	-	
			@100kHz	24	-	-	
			@1MHz	45	-	-	
Input logic-level high	V_{IH}	For digital inputs		0.9V_{DD12}	-	V_{DD12}+0.3	V
Input logic-level low	V_{IL}			-0.3	-	+0.3	V