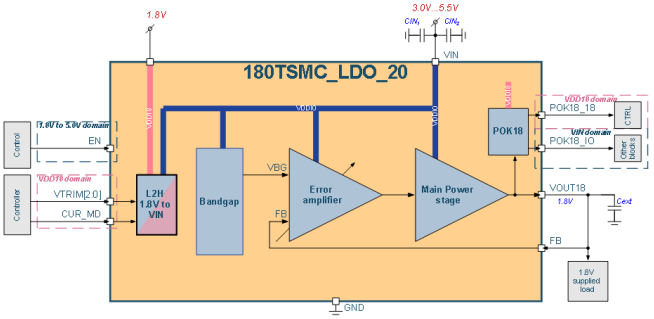
40 mA LDO voltage regulator (3.0/5.5V to 1.8V)

OVERVIEW

180TSMC_LDO_20 is LDO to convert IO voltage 3.0V÷5.5V to 1.8V and designed to supply integrated circuits with stable and precise voltage with load up to 40mA.
The output voltage can be fine-tuned from +3% to -4% at nominal value.
The main feature of this LDO is ultra-low power consumption 1.2uA@VIN=5.0V at 5mA load current.



IP includes Bandgap voltage reference source as well as supplies LDO sub-blocks by PTAT reference current. There is Power-OK circuit to indicate a status about output voltage.

IP technology: TSMC 180nm CMOS.
IP status: silicon proven.
Silicon area: 0.181mm^2

ELECTRICAL CHARACTERISTICSДА

Parameter	Symbol	Conditions		Value			Unit
				min	typ.	max	
Analog supply voltage	VIN	-		2.7	3.0	3.3	V
		-		4.95	5.5	6.05	
Digital supply voltage	VDD18	For level converters		1.7	1.8	1.9	V
Operating junction temperature	T_j	-		-40	+27	+125	°C
Input logic-level high	V_{IH}	For digital inputs		VDD18-0.25	-	VDD18	V
Input logic-level low	V_{IL}			0	-	0.25	V
External load capacitor	C_{load}	-		1.0	2.2	-	µF
Maximum load current	I_{load}	-		-	-	40	mA
Quiescent current	I_Q	Tj=-40÷125°C, IOUT = 5mA, VIN = 5.0V	Normal mode	-	1.2	2.1	µA
			Boost mode	-	5.9	10.3	µA
EN input current	I_{CC_EN}	Tj=-40÷125C, EN=5.5V		-	80	140	nA
Shutdown current	I_{STD}	EN = "0"		-	2.2	115	nA
Regulated output voltage	VOUT18	IOUT = 30mA,VIN = 5.0V		1.7	1.81	1.9	V
Load regulation	LDR	IOUT = 1µA ÷ 40mA, VIN=5V		-	-	0.6	V/A
Line regulation	LNR	IOUT = 30mA, VIN= 4.0V to 5.0V, Tj =-40°C÷+125°C		-	0.17	0.3	%/V
Load transient response (Undershoot)	ΔV_{OLD}	IOUT = 10µA –> 20mA (undershoot), (Rise Time=1us), VIN=5V	Normal mode	-	-	-0.22	V
			Boost mode	-	-	-0.12	V
Load transient response (Overshoot)	ΔV_{OLD}	IOUT = 20mA –> 10µA (undershoot) (Fall Time=1us), VIN=5V	Normal mode	-	-	+0.18	V
			Boost mode	-	-	+0.07	V