1.25 Gbps LVDS IPs library

OVERVIEW

028TSMC_LVDS_01 is a library including:

- Transmitter LVDS driver (TX_LVDS);
- Receiver LVDS driver (RX_LVDS);
- Reduced range link receiver LVDS driver (RX_LVDS_R);
- Transceiver LVDS driver (RX_TX_LVDS);
- Reference current/voltage generators (RS_TOP);
- Bias block (LVDSBIAS8X) for 8 LVDS drivers

RX_TX_LVDS driver has five available operation modes: transmitter, receiver, transmitter half-duplex, receiver half-duplex and shutdown. The RS_TOP block is intended to output reference currents and voltage for RX_LVDS, RX_LVDS_R, TX_LVDS and TX_RX_LVDS drivers as well as for bias block. Composing of LVDS library components allows to design a device with up to 16 pairs of data channels and 2 pairs of synchronization channels.

Features:

- TIA/EIA-644 LVDS standards without hysteresis
- Data transfer rate: 1250Mbps
- 1.8V IO voltage supply
- 0.9V core voltage supply
- 0.9V CMOS input/output logic control signals
- 0.9V/1.8V level shifters
- TSMC 28nm CMOS technology

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

BLOCK DIAGRAM

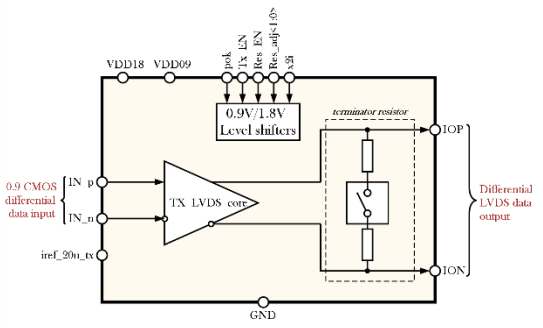

Figure 1: **TX_LVDS** driver block diagram

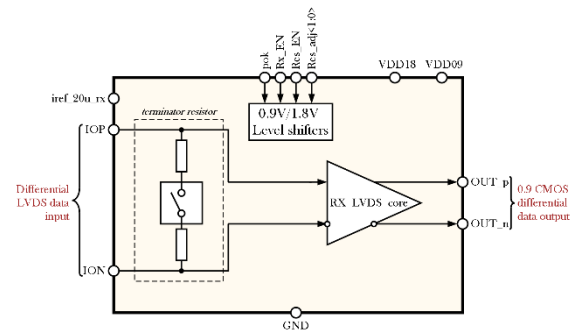

Figure 2: **RX_LVDS** driver block diagram

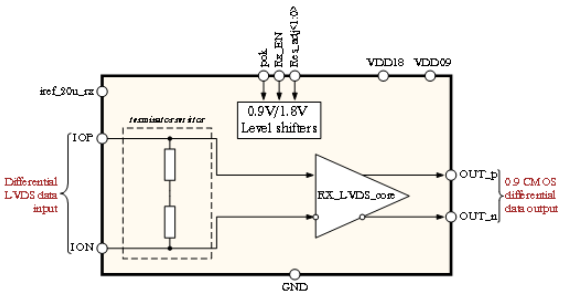

Figure 3: **RX_LVDS_R** driver block diagram

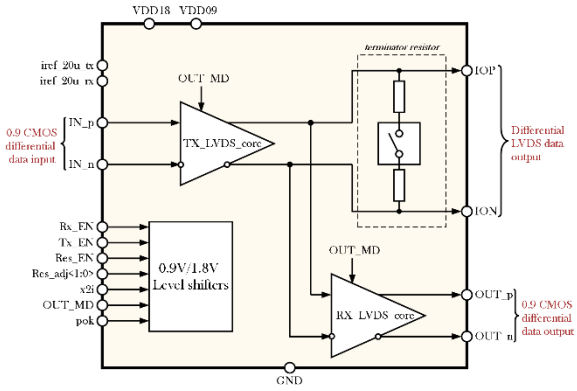

Figure 4: **RX_TX_LVDS** driver block diagram

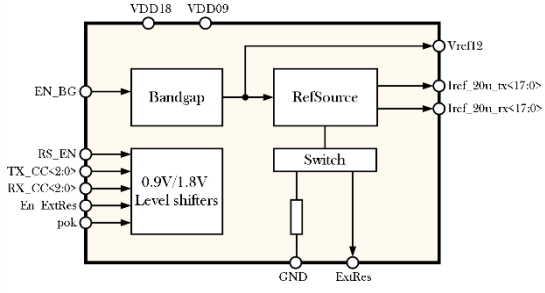

Figure 5: **RS_TOP** block diagram

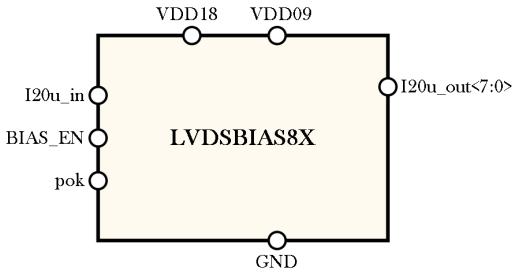

Figure 6: **LVDSBIAS8X** block diagram