7.5 Gbps DDR CML IPs library

OVERVIEW

040TSMC_CML_01 is a library including:

- CML receiver (CML_RX);
- CML transmitter (CML_TX).
- Reference current/voltage source (CML_RS);
- Reference current/voltage buffer (CML_BIAS).

The CML_RX block is intended to receive a CML signal and convert it to a CMOS signal. The CML_TX block is intended to convert signal from CMOS to CML standard and transmit CML signal to external circuits. CML_TX has pre-emphasis circuit.

The CML_RS block is intended to output reference currents and voltage for drivers, as well as for Bias block. CML_BIAS is used to buffer and split reference currents between the receiver and transmitter channels.

Area:

- CML_RX – 0.025mm^2;
- CML_TX – 0.063mm^2;
- CML_RS – 0.053mm^2;
- CML_BIAS – 0.011mm^2.

IP technology: TSMS 40nm LP technology.
IP status: pre-silicon verification

Features:

- 2.5V IO voltage supply
- 1.1V core voltage supply
- 1.1V CMOS input/output logic control signals
- 1.1V/2.5V level shifters
- Data transfer rate: 3.75 GHz / 7.5Gbps (DDR MODE) switching rates
- 1 CML RX driver and 1 CML TX driver, scalable up to number, requested by Customer
- Temperature range: -40 °C to +125 °C
- TSMC 40nm LP process

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

BLOCK DIAGRAM

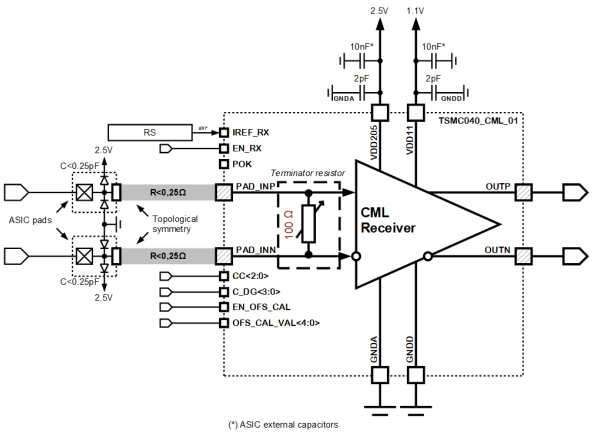

Figure 1 CML_RX block diagram

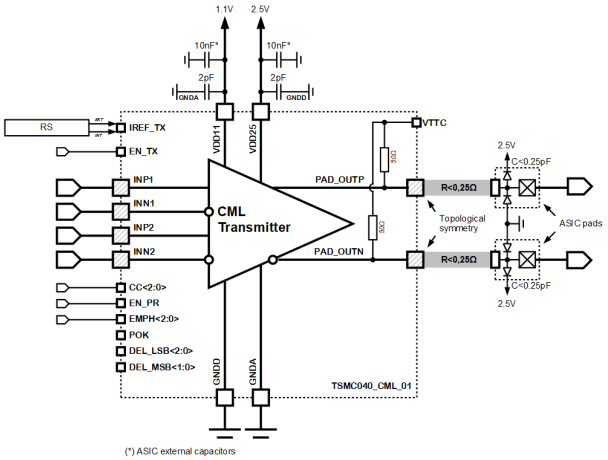

Figure 2 CML_TX block diagram

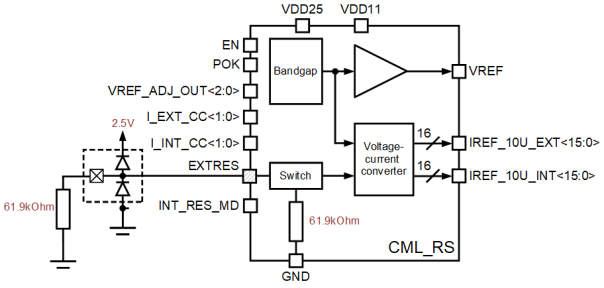

Figure 3 CML_RS block diagram

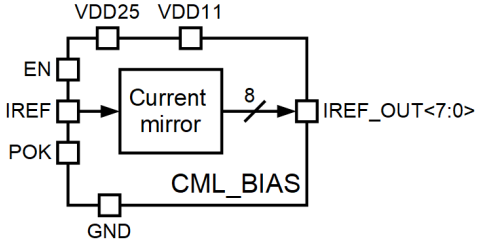

Figure 4 CML_BIAS block diagram