4 Gbps DDR CML receiver and transmitter

OVERVIEW

055TSMC_CML_01 is a library including:

- CML receiver (CML_RX);
- CML transmitter (CML_TX).

The CML_RX block is intended to receive a CML signal and convert it to a CMOS signal. The CML_TX block is intended to convert signal from CMOS to CML standard and transmit CML signal to external circuits. CML_TX has pre-emphasis circuit.

IP technology: TSMC 55nm CMOS EF technology.

IP status: pre-silicon verification.

Total silicon area:

- CML_RX – 0.012mm^2;
- CML_TX – 0.015mm^2.

Features:

- TIA/EIA-644 LVDS standards
- Data rate (receive/transmit): up to 4 Gbps (DDR mode)
- 1.2V digital voltage supply
- 1.2V core voltage supply
- 1.2V CMOS input/output logic control signals
- Temperature range: -40 °C to + 85 °C

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

BLOCK DIAGRAM

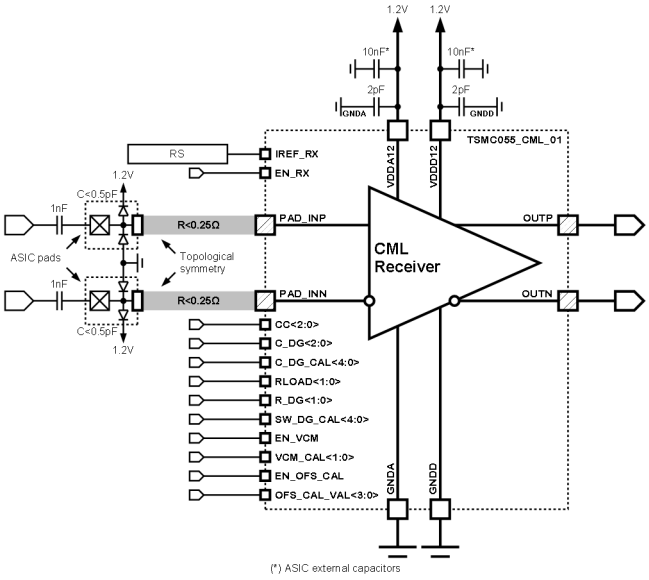

Figure 1 CML_RX block diagram

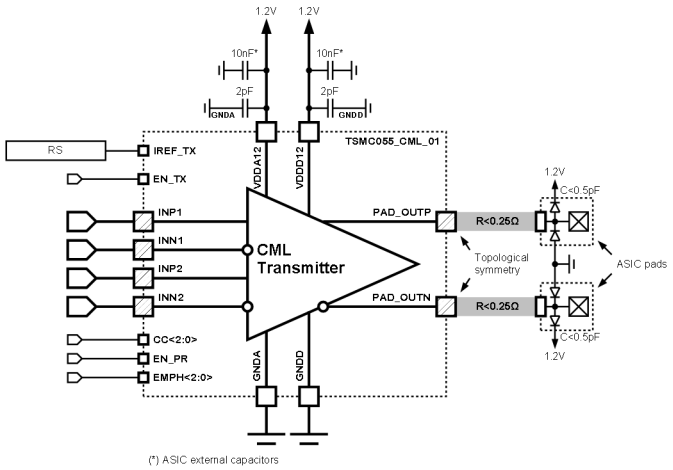

Figure 2 CML_TX block diagram