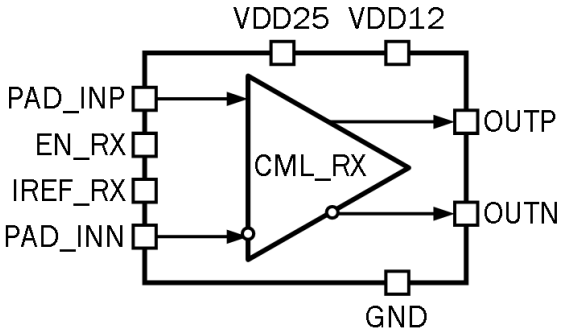
3.125 Gbps DDR CML receiver

OVERVIEW

065TSMC_CML_01 core logic interface includes complementary output signal pins (**OUTp**, **OUTn**) for data transmission and enable pin **EN_RX. PAD_INP** and **PAD_INN** are differential input pins that should be connected to bonding pads. Buffer includes two 50-Ohm on-chip termination resistors, connected to supply voltage node. So the interface supports both AC and DC-coupled connections. **IREF_RX** is a reference current input.
IP technology: TSMC CMOS 65nm.
IP status: silicon proven.
Area: 0.0048mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply digital voltage	V_{DD12}	-	1.14	1.2	1.26	V
	V_{DD25}	-	2.375	2.5	2.625	
Operating temperature range	T_j	-	-40	+85	+125	°C
Input reference current	I_{REF_RX}	-	-	40	-	uA
Input voltage range	V_{in}	-	1.14	1.2	1.26	V
Input differential threshold	V_{th}	-	100	400	-	mV
Data rate	F_S	DDR mode	-	3.125	-	Gbps
DC current consumption	I_{VDD25}	IREF_RX=40uA	-	1	1.1	mA
Stand-by current	I_{st}	-	136	382	432	nA
Output voltage range	V_{OUT}	-	0	-	1.25	V
Differential time propagation delay	t_{PHLDT}	High to low	638.7	648.3	652.3	ps
	t_{PLHDT}	Low to high	634.8	646.1	657.4	ns
AC current consumption	I_{VDD25}	-	1.20	1.37	1.40	mA
Total AC power consumption	P	-	1.37	1.64	1.76	mW
Clock jitter, random rms	t_{RJ}	Ampl_in = 0.12 V	1.10	1.57	2.65	ps
Clock jitter, random max (p-p)	t_{DJM}		1.55	2.21	3.74	ps
Input voltage high level	V_{IH}	For digital inputs	$0.8V_{DD12}$	-	V_{DD12}	V
Input voltage low level	V_{IL}		0	-	$0.2V_{DD12}$	V