CML Transmitter

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- 1.2 V digital power supply
- 1.2 V CMOS input logic signals
- 8-step (3-bit) adjustable transmitter output current (range from 4 mA to 32 mA)
- 3.125 Gbps (DDR MODE) switching rates
- Temperature range: -40 °C to +125 °C
- Portable to other technologies (upon request)

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

3 OVERVIEW

Core logic interface includes signal pins (INp1, INp2 and INn1, INn2) for data transmission, control pin EN_TX to configure transmitter state and control pin EN_PR to toggle pre-emphasis mode. Data on signal pins INp2 and INn2 should be one bit shifted (delayed) from that on INp1 and INn1 for pre-emphasis purposes. IREF_TX is a reference current input. Differential CML output pins PAD_OUTp and PAD_OUTn should be connected to bonding pads.
CML transmitter is designed on TSMC CMOS 65nm technology.

4 STRUCTURE

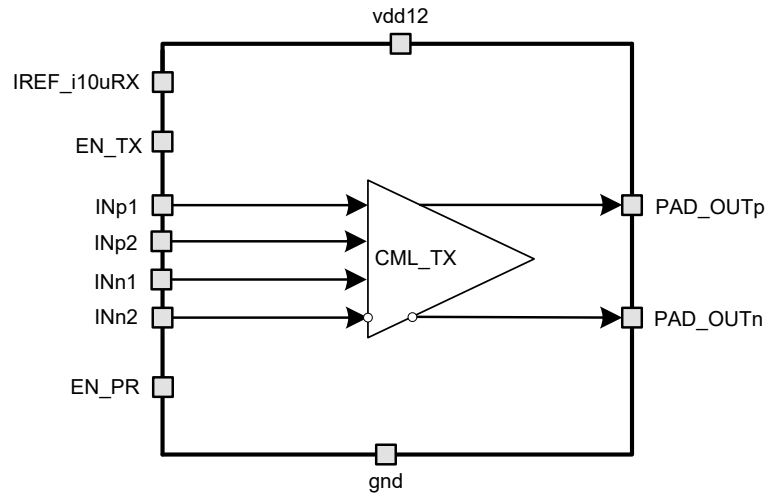

Figure 1: CML transmitter structure.

5 PIN DESCRIPTION

Name	Direction	Description
IREF_i10uTX	I	Reference current 10 uA
EN_TX	I	CML transmitter enable
EN_PR	I	CML pre-emphasis enable
INp1	I	Input complementary CMOS signals
INn1	I	
INp2	I	Input complementary CMOS signals, one bit shifted
INn2	I	
PAD_OUTp	O	Output differential CML signal of transmitter
PAD_OUTn	O	
vdd12	IO	Supply voltage 1.2 V
gnd	IO	Ground

Table 1: CML transmitter truth table.

Mode	Input		Output	
	EN_TX	INp	PAD_OUTp	PAD_OUTn
Transmit	1	0	0	1
		1	1	0
Power down	0	X	Z	Z

6 LAYOUT DESCRIPTION

CML transmitter dimensions are given in the table 2.

Table 2: Block dimensions.

Dimension	Value	Unit
Height	176	um
Width	196	um

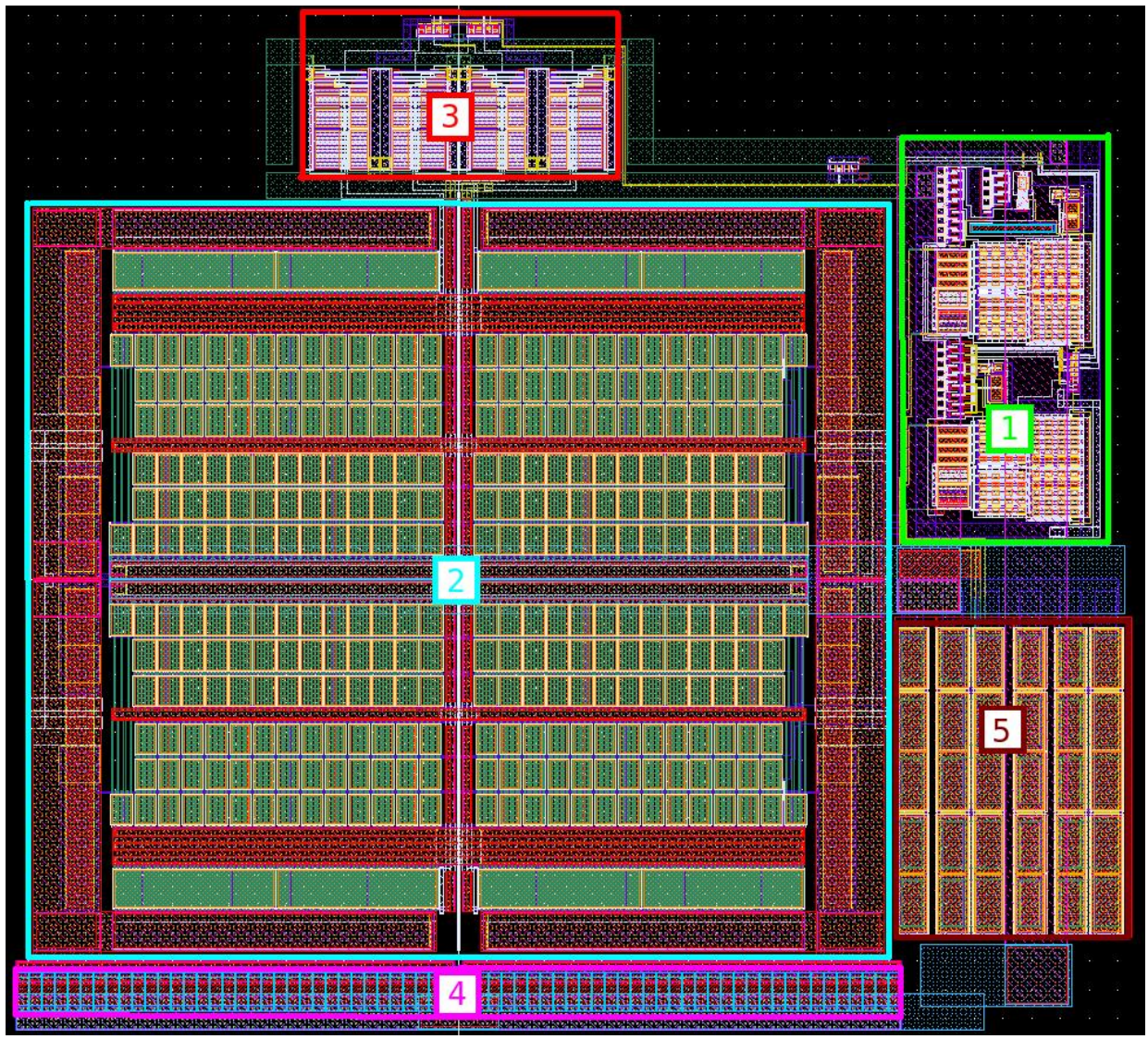

Figure 2: CML transmitter layout view.

1. Reference bias
2. Output stage
3. Digital buffers
4. Internal terminator
5. Filtering capacitor for bias voltage

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65 nm
Status _____ silicon proven
Area _____ 0.35 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd12}= 1.14 ÷ 1.26 and T = -40 ÷ +125 °C, R_L=50Ω (load resistance). Typical values are at V_{dd12}= 1.2V, T= +85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply digital voltage	V_{dd12}	-	1.14	1.2	1.26	V
Operating temperature range	T	-	-40	+85	+125	°C
Differential output voltage	V_{OD}	EN_PR = "0"	400	800	1600	mV
		EN_PR = "1"	400	800	1800	mV
Output offset voltage	V_{OS}	-	0.8	1	1.1	V
|Change V_{OD}|	ΔV_{OD}	-	-	-	50	mV
|Change V_{OS} |	ΔV_{OS}	-				
Stand-by current	I_{st}	-	-	-	2	µA
Input voltage range	V_{in}	-	0	-	1.2	V
Output current	I_{out}	IREF_i10uTX=10µA	-	16	-	mA
DC power current from V_{dd} random data without output current	I_{VDD}	IREF_i10uTX=10 µA EN_PR = "0"	1.9	2	2.1	mA
		IREF_i10uTX=10µA EN_PR = "1"	4.4	4.5	4.6	mA
Total power without output current	P_{total}	IREF_i10uTX=10µA EN_PR = "0"	2.18	2.4	2.62	mW
		IREF_i10uTX=10µA EN_PR = "1"	5.06	5.4	5.75	mW
Differential time propagation delay, high to low	t_{PHLDT}	-	160	225	275	ps
Differential time propagation delay, low to high	t_{PLHDT}					
Rise time	t_{RT}	C_L=1p	-	-	100	ps
Fall time	t_{FT}		-	-	100	ps
AC power current from V_{dd}	I_{VDD}	-	32.6	37.76	45.4	mA
Total AC power	W	-	37.5	45.31	56.72	mW
Clock jitter, random rms	t_{RJ}	C_L=1p	78	100	240	fs
Clock jitter, random max (p-p)	t_{DJM}		0.42	0.88	1.33	ps
Data jitter, deterministic	t_{DJ}		0.42	0.88	1.33	ps
Duty cycle	S	-	48	49	50	%
Input voltage high level	V_{IH}	For digital inputs	0.8V_{dd12}		V_{dd12}	V
Input voltage low level	V_{IL}	For digital inputs	0		0.2 V_{dd12}	V

8 TYPICAL CHARACTERISTICS

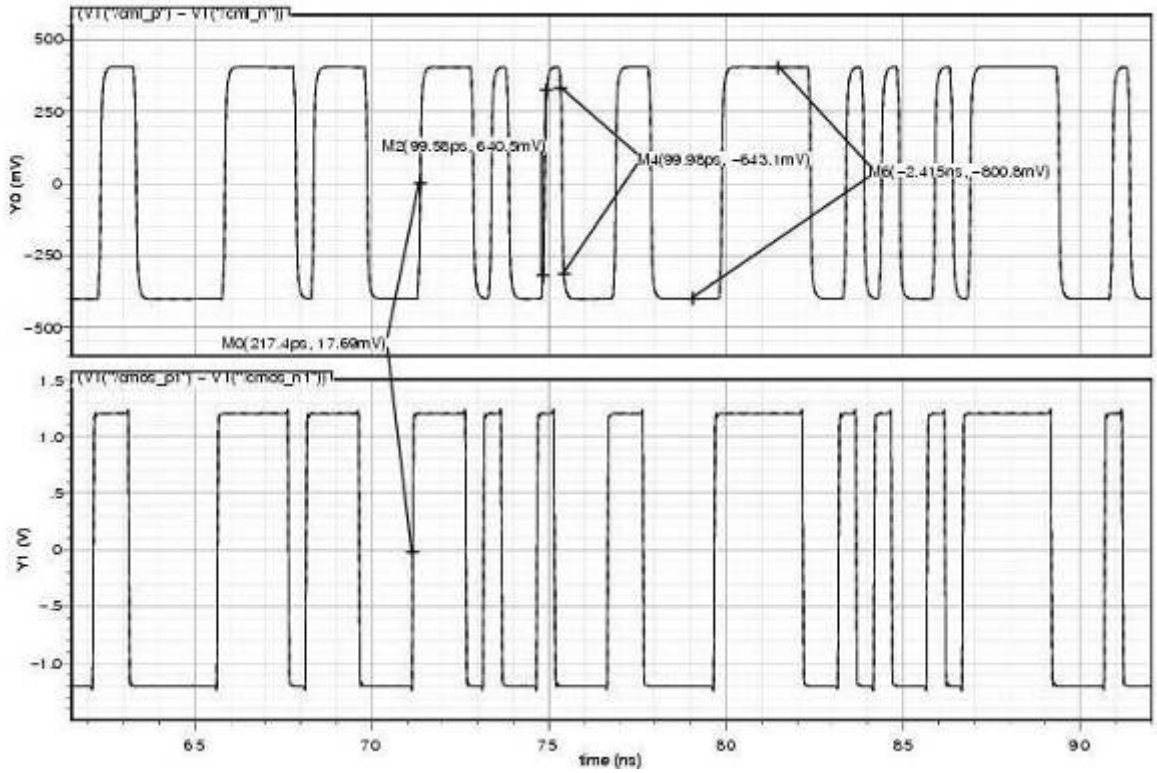

Figure 3: The time diagram of the transmitter at a frequency of 2 GHz.

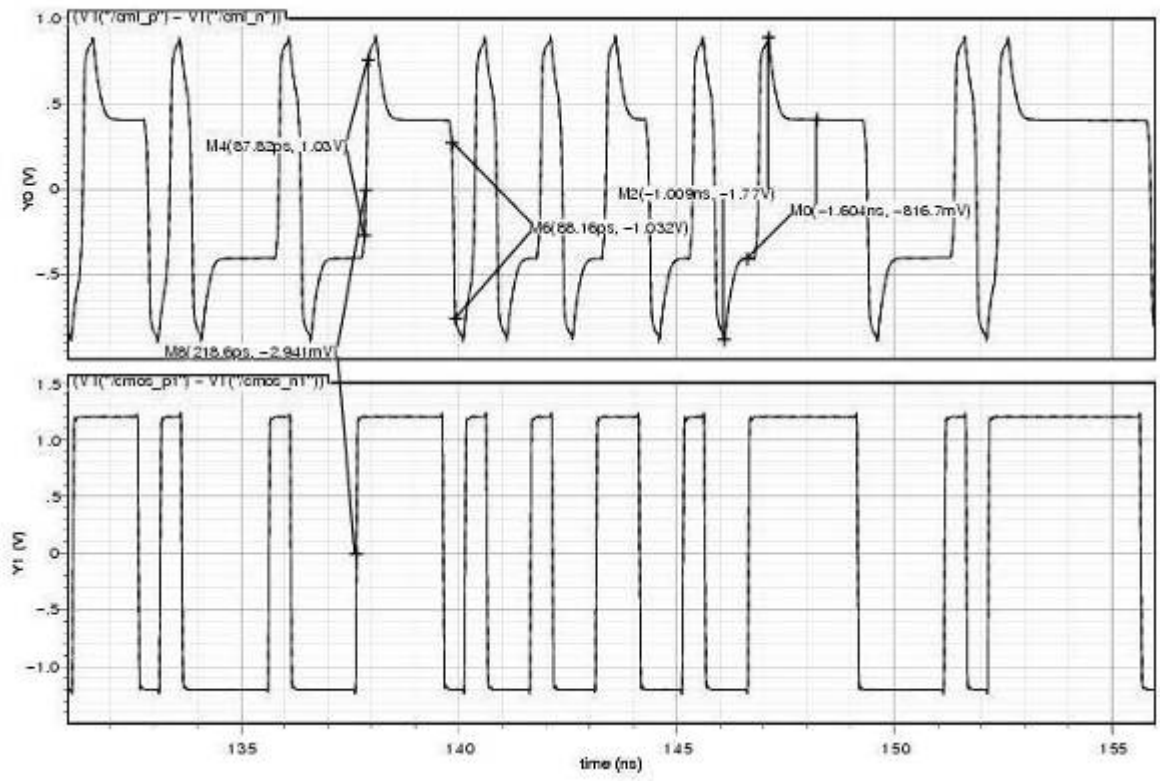

Figure 4: The time diagram of the transmitter at a frequency of 2 GHz with preemphasis.

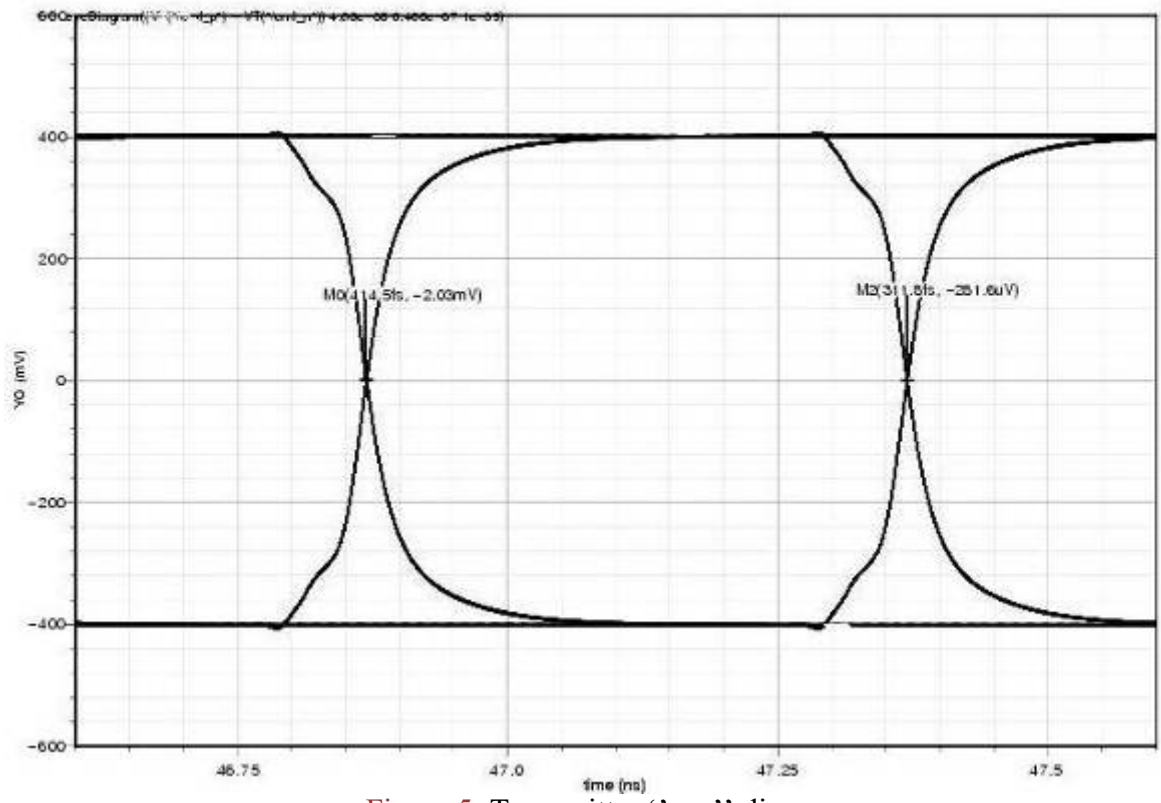

Figure 5: Transmitter ‘’eye’’ diagram.

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation