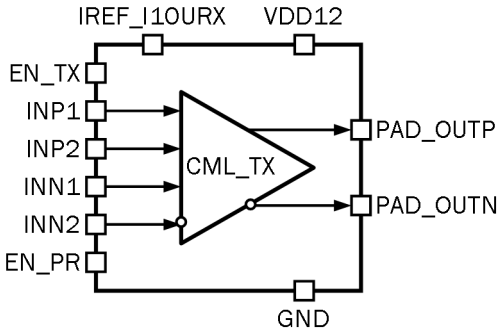
3.125 Gbps DDR 1-channel CML transmitter

OVERVIEW

065TSMC_CML_02 core logic interface includes signal pins (**INP1**, **INP2** and **INN1**, **INN2**) for data transmission, control pin **EN_TX** to configure transmitter state and control pin **EN_PR** to toggle pre-emphasis mode. Data on signal pins **INP2** and **INN2** should be one bit shifted (delayed) from that on **INP1** and **INN1** for pre-emphasis purposes. Differential CML output pins **PAD_OUTP** and **PAD_OUTN** should be connected to bonding pads.

IP technology: TSMC CMOS 65nm.
IP status: silicon proven.
Area: 0.035mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				min	typ.	max	
Supply digital voltage	V_{DD12}	-		1.14	1.2	1.26	V
Operating temperature range	T	-		-40	+85	+125	°C
Input reference current	I_{REF}	-		-	10	-	uA
Differential output voltage	V_{OD}	EN_PR = "0"		400	800	1600	mV
		EN_PR = "1"		400	800	1800	mV
Output offset voltage	V_{OS}	-		0.8	1	1.1	V
|Change V_{OD}|	ΔV_{OD}	-		-	-	50	mV
|Change V_{OS}|	ΔV_{OS}	-					
Stand-by current	I_{st}	-		-	-	2	uA
Input voltage range	V_{in}	-		0	-	1.2	V
Data rate	F_S	DDR mode		-	3.125	-	Gbps
Output current	I_{out}	IREF_I10UTX=10uA		-	16	-	mA
DC current consumption from VDD random data without output current	I_{VDD}	IREF_I10UTX=10uA	EN_PR = "0"	1.9	2	2.1	mA
			EN_PR = "1"	4.4	4.5	4.6	mA
Total power without output current	P_{total}	IREF_I10UTX=10uA	EN_PR = "0"	2.18	2.4	2.62	mW
			EN_PR = "1"	5.06	5.4	5.75	mW
Differential time propagation delay	t_{PHLDT}	High to low		160	225	275	ps
	t_{PLHDT}	Low to high					
Rise time	t_{RT}	C_L=1pF		-	-	100	ps
Fall time	t_{FT}			-	-	100	ps
AC current consumption from V_{DD}	I_{VDD}	-		32.6	37.76	45.4	mA
Total AC power	W	-		37.5	45.31	56.72	mW
Clock jitter, random rms	t_{RJ}	C_L=1pF		78	100	240	fs
Clock jitter, random max (p-p)	t_{DJM}			0.42	0.88	1.33	ps
Data jitter, deterministic	t_{DJ}			0.42	0.88	1.33	ps
Duty cycle	S	-		48	49	50	%
Input voltage high level	V_{IH}	For digital inputs		$0.8V_{DD12}$	-	V_{DD12}	V
Input voltage low level	V_{IL}			0	-	$0.2V_{DD12}$	V