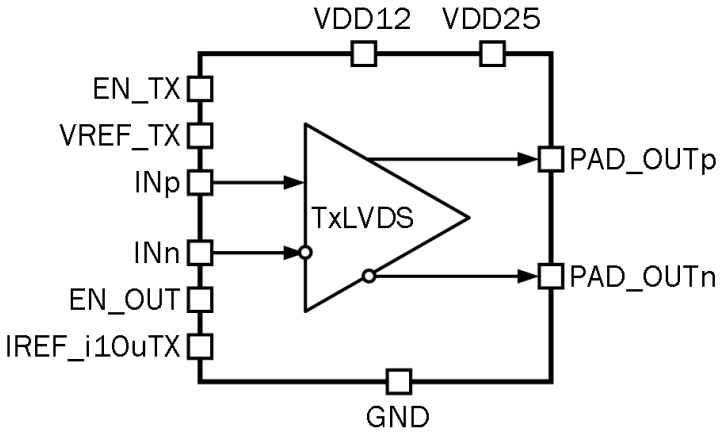
1 Gbps DDR LVDS transmitter

OVERVIEW

065TSMC_LVDS_05 includes signal pins (**INp** and **INn**) to transmit data, and control pin **EN_TX** to configure the state of the transmitter. There are other two internal pins (**VREF_TX** and **IREF_TX**) to get voltage reference and current reference. **PAD_OUTp** and **PAD_OUTn** are complementary outputs to connect to the bonding pads. The block conforms to TIA/EIA-644 LVDS standards without hysteresis.

IP technology: TSMC 65nm CMOS.
IP status: silicon proven.
Area without PADs: 0.015mm^2.
Area with PADs: 0.045mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Analog supply voltage	V_{DD25}	-	2.375	2.5	2.625	V
Digital supply voltage	V_{DD12}	-	1.14	1.2	1.26	V
Operating temperature range	T	-	-40	+85	+125	°C
Differential output voltage	V_{OD}	-	300	350	400	mV
Output offset voltage	V_{OS}	-	1.125	1.250	1.375	V
Differential time propagation delay, high to low	t_{PHLDT}	-	1	1.4	1.6	ns
Differential time propagation delay, low to high	t_{PLHDT}					
Output current	I_{OUT}	IREF_TX = 10uA	-	3.5	-	mA
Rise time	t_{RT}	C_{LOAD}=1pF	330	340	350	ps
Fall time	t_{FT}		330	340	350	ps
Data rate		DDR mode	-	-	1	Gbps
AC power current from V_{dd25}	I_{VDD25}	IREF_TX = 10uA	16.0	21.4	25.2	mA
AC power current from V_{dd12}	I_{VDD12}		0.35	0.35	0.37	mA
Total AC power	W		38.7	53.3	65.5	mW
Clock jitter, rms	t_{RJ}	C_{LOAD}=1pF	300	400	900	fs
Data jitter, deterministic	t_{DJ}		0.8	1.3	6.0	ps
Duty cycle	S	-	49	50	51	%
Input voltage high level	V_{IH}	For digital inputs	$0.8V_{DD12}$	-	V_{DD12}	V
Input voltage low level	V_{IL}		0	-	$0.2V_{DD12}$	V