Rail to Rail LVDS Receiver

SPECIFICATION

1 FEATURES

- TSMC CMOS 0.065 um
- 2.5 V analog power supply
- 1.2 V digital power supply
- 1.2 V CMOS input and output logic signals
- 1 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards without hysteresis
- Rail to rail input range
- Temperature range: -40 °C to + 125 °C
- Optimized for pad-limited layout design
- Portable to other technologies (upon request)

2 APPLICATION

- Point-to-point data receiver
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data receiver
- Cable data receiver

3 OVERIVIEW

LVDS_RX is LVDS receiver with rail to rail input range. The interface to the core logic includes the output signal pins (OUTp, OUTn) to receive data and the control pins (EN_RX, EN_RES) to configure the state of the receiver. EN_RES enables the on-chip 100 ohm resistor. The VREF12 is input voltage reference. Pin IREF_RX to get current reference from receiver bias. PAD_INp and PAD_INn are complementary input to connect to the bonding pads.

4 STRUCTURE

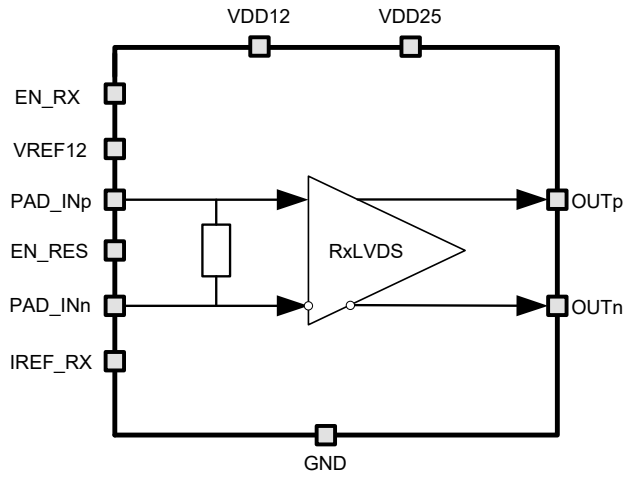

Figure 1: Rail to Rail LVDS Receiver structure.

5 PIN DESCRIPTION

Name	Direction	Description
IREF_RX	I	Reference current
VREF12	I	Reference voltage
EN_RES	I	On-chip resistor enable
EN_RX	I	LVDS receiver enable
PAD_INp	I	Input differential LVDS signal
PAD_INn		
OUTp	O	Output differential CMOS signal
OUTn		
VDD12	IO	Supply voltage 1.2 V
VDD25	IO	Supply voltage 2.5 V
GND	IO	Ground

Table 1: LVDS receiver truth table.

Mode	Input			Output	
	EN_RX	PAD_INp	PAD_INn	OUTp	OUTn
Receive	1	1	0	1	0
		0	1	0	1
Power down	0	X	X	0	0

6 LAYOUT DESCRIPTION

Rail to Rail LVDS Receiver dimensions are given in the table 2.

Table 2: Block dimension.

Dimension	Value	Unit
Height	88	um
Width	145	um

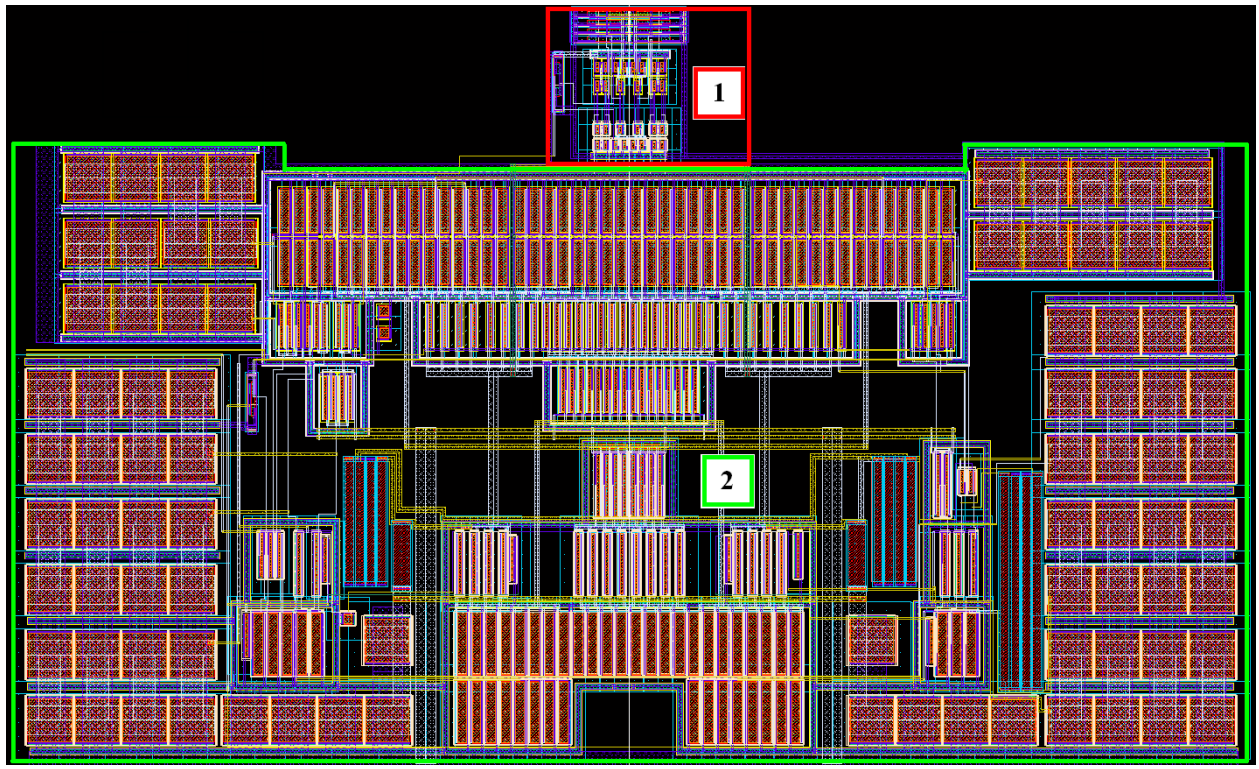

Figure 2: Rail to rail LVDS Receiver layout view.

1. Digital buffer
2. Rail to rail LVDS receiver

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 0.65um
Status _____ silicon proven
Area _____ 0.06 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd25} = 2.375 ÷ 2.625 V, V_{dd}= 1.14÷ 1.26, T = -40 ÷+125 °C. Typical value are at V_{dd25}= 2.5V, V_{dd}= 1.2V, T=+ 85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply analog voltage	V_{dd25}	-	2.375	2.5	2.625	V
Supply digital voltage	V_{dd}	-	1.14	1.2	1.26	V
Operating temperature range	T	-	-40	+85	+125	°C
Input voltage range (common-mode)	V_{in}	-	0	1.25	2.5	V
Input differential threshold	V_{th}	-	-	100	-	mV
DC power current from V_{dd25}	I_{VDD25}	IREF_RX=30uA	1.18	1.6	1.87	mA
		IREF_RX=60uA	2.09	3.02	3.73	mA
Total power	P_{total}	IREF_RX=30uA	2.95	4.00	4.68	mW
		IREF_RX=60uA	5.23	7.55	9.33	mW
Stand-by current	I_{st}	-	1.63	21.1	85.5	nA
Output voltage range	V_{out}		0	-	1.2	V
Differential time propagation delay, high to low	t_{PHLDT}	-	0.00	1.02	1.13	ns
Differential time propagation delay, low to high	t_{PLHDT}	-	0.94	0.98	1.09	ns
AC power current from V_{dd25}	I_{VDD25}	IREF_RX=30uA	1.97	2.46	2.7	mA
Total AC power	W	IREF_RX=30uA	4.93	6.15	6.75	mW
Clock jitter, rms	t_{RJ}	Without load	1.50	1.80	2.30	ps
Clock jitter, max (p-p)	t_{DJM}		2.04	2.27	2.90	ps
Data jitter, deterministic	t_{DJ}		12.4	12.7	13.7	ps
Input voltage high level	V_{IH}	For digital inputs	0.8 V_{dd25}	-	V_{dd25}	V
Input voltage low level	V_{IL}	For digital inputs	0	-	0.2 V_{dd25}	V

8 TYPICAL CHARACTERISTICS

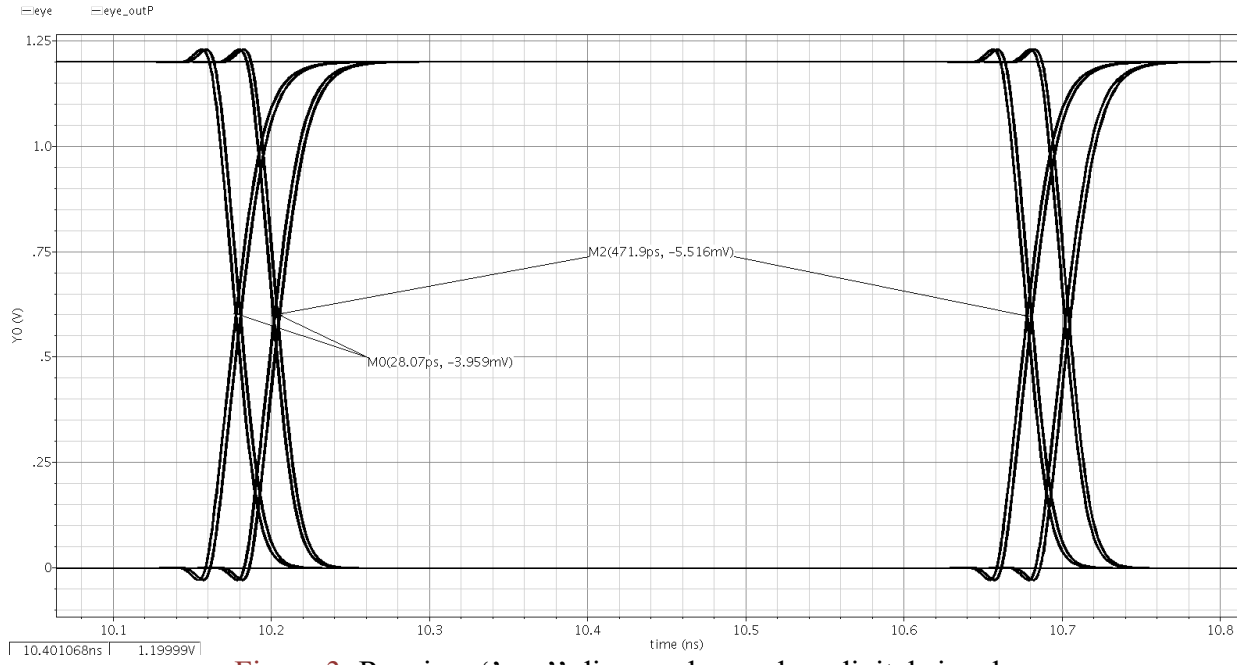

Figure 3: Receiver ‘’eye’’ diagram by random digital signal.

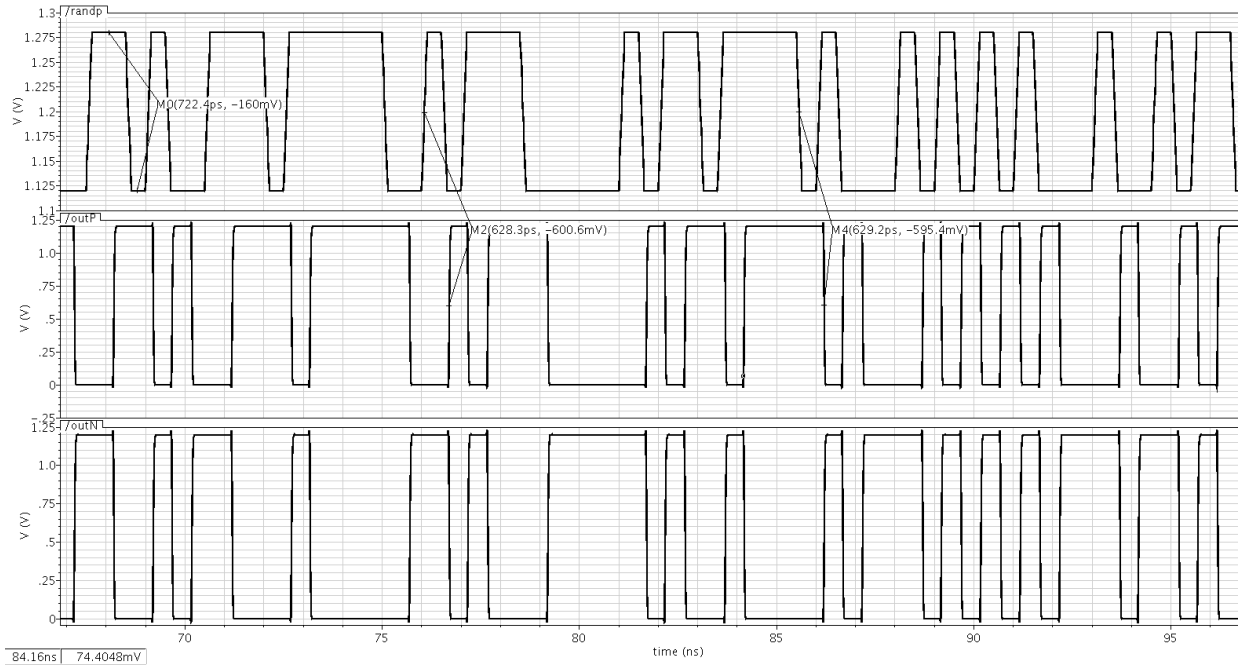

Figure 4: The time diagram of the receiver by a random digital signal.

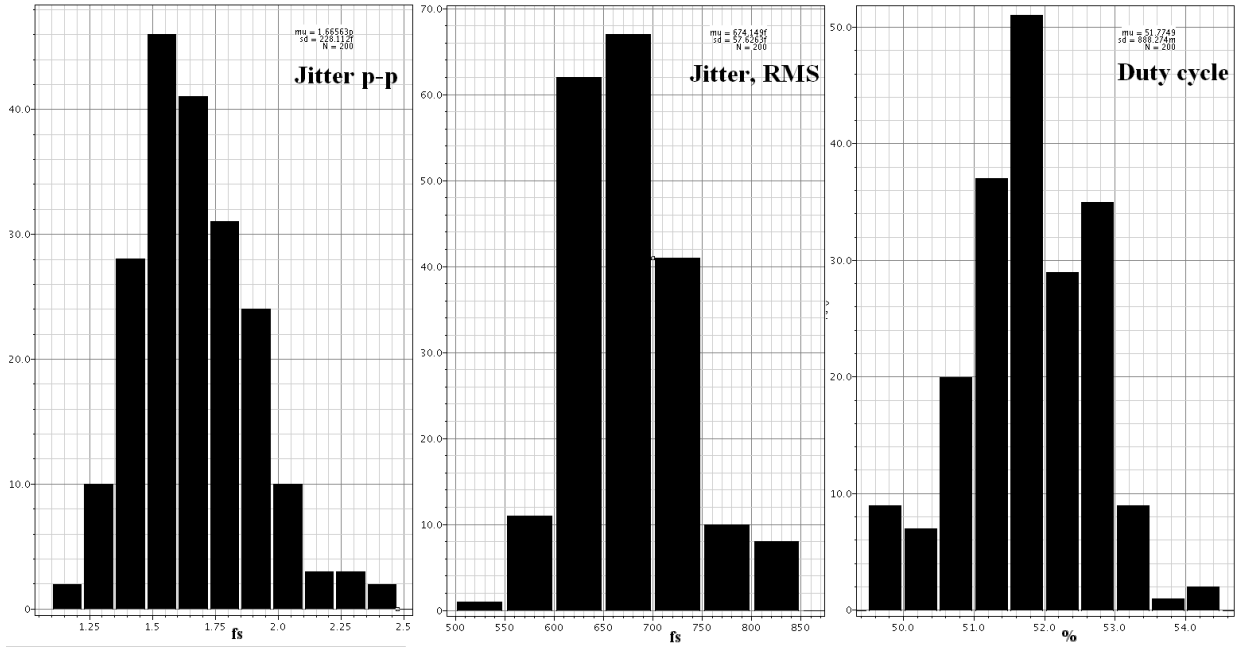

Figure 5: The results of statistical analysis.

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation