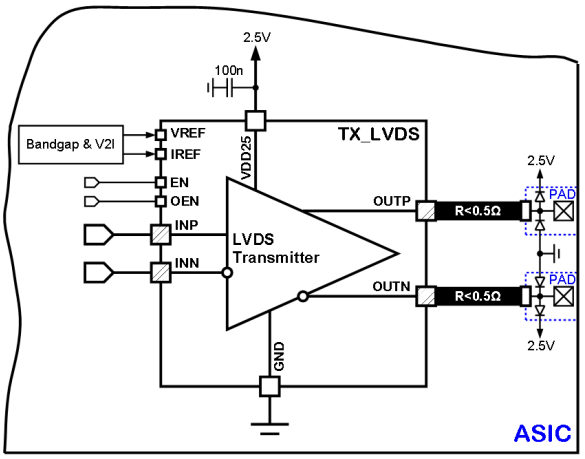
2.4 Gbps DDR LVDS transmitter

OVERVIEW

065TSMC_LVDS_07 is LVDS transmitter. The interface to the core logic includes differential signal pins (**INP** and **INN**) to transmit data, and control pin **EN** to configure the state of the transmitter. EN pin enables of the TX LVDS, **OEN** pin selects Hi-Z state mode in which the output is disconnected. There are other two internal pins (**VREF** and **IREF**) to get voltage reference and current reference. **OUTP** and **OUTN** are complementary outputs to connect to the bonding pads.



IP technology: TSMC CMOS 65nm.
IP status: pre-silicon verification.
Area: 0.015mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				min	typ.	max	
Supply analog voltage	V_{DD25}	-		2.25	2.5	2.75	V
Operating temperature range	T_j	-		-45	+27	+85	°C
Input reference current	I_{REF}	-		-	10	-	uA
Input reference voltage	V_{REF}	-		-	1.2	-	V
Differential output voltage	V_{OD}	I_{REF} = 10uA, R_L=100±1%		282	350	390	mV
Output offset voltage	V_{OS}	(V_{OUTP} + V_{POUTN})/2		1.165	1.2	1.235	V
Differential time propagation delay	t_{PHL}	C_L=1pF	high to low	0.45	0.6	0.83	ns
	t_{PLH}		low to high				
Differential skew	t_{skew1}	Between t_{PHL} and t_{PLH}		-	9	21	ps
Line short circuit current	I_{sa},I_{sb}	V_{OUTP} and V_{OUTN} shorted to ground		-	10.3	11.5	mA
Pair short circuit current	I_{sab}	V_{OUTP} shorted to V_{OUTN}		-	3.5	3.9	mA
Stand-by current	I_{st}	-		-	-	74	nA
DC power current from V_{DD25}	W_{DC}	I_{REF} = 10uA, R_L=100±1%		3.12	3.8	4.2	mA
Total DC power	P_{total}	I_{REF} = 10uA, R_L=100±1%		7	9.5	11.5	mW
Rise time	t_{RT}	C_L=1pF		60	71	94	ps
Fall time	t_{FT}			60	71	94	ps
AC power current from V_{DD25}	I_{VDD25}	I_{REF} = 10uA		8.7	9.9	11.2	mA
Total AC power	W_{AC}			19.6	24.7	30.8	mW
Clock jitter, rms	t_{RJ}	C_L=1pF		40	63	110	fs
Clock jitter, max (p-p)	t_{DJM}			0.25	0.4	0.68	ps
Data jitter, deterministic	t_{DJ}			0.3	0.4	1	ps
		C_L=3pF		9	10	11	ps
Data jitter, deterministic crossing ±100mV	t_{DJC}	C_L=1pF		26	27	28	ps
		C_L=3pF		95	95	112	ps
Duty cycle	S	-		49	50	51	%
Input voltage high level	V_{IH}	For digital inputs		0.8V_{DD25}	-	V_{DD25}	V
Input voltage low level	V_{IL}			0	-	0.2V_{DD25}	V