1 Gbps rail to rail LVDS receiver

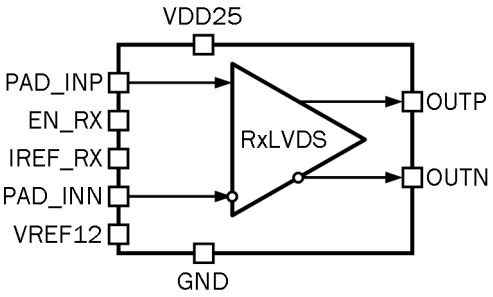
OVERVIEW

065TSMC_LVDS_08 is LVDS receiver with rail to rail input range. The interface to the core logic includes the output signal pins (**OUTP**, **OUTN**) to receive data and the control pin **EN_RX** to configure the state of the receiver. The **VREF12** pin is input voltage reference. Pin **IREF_RX** to get current reference from receiver bias. **PAD_INP** and **PAD_INN** are complementary input to connect to the bonding pads. This LVDS receiver does not employ hysteresis, and therefore does not comply with the hysteresis requirement of the TIA and IEEE standards for LVDS differential signaling at the specified rates.

IP technology: TSMC CMOS 65nm.

IP status: silicon proven.

Area: 0.01mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply analog voltage	V_{DD25}	-	2.375	2.5	2.625	V
Operating temperature range	T_j	-	-40	+85	+125	°C
Input reference voltage	V_{REF}	-	-	1.2	-	V
Input reference current	I_{REF}		-	30	-	uA
Input voltage range (common-mode)	V_{in}	-	0	1.25	2.5	V
Input differential threshold	V_{th}	-	-	-	100	mV
DC power current from V_{DD25}	I_{VDD25}	-	1.18	1.6	1.87	mA
Total power	P_{total}	-	2.95	4.00	4.68	mW
Stand-by current	I_{st}	-	1.63	21.1	85.5	nA
Output voltage range	V_{out}	-	0	-	1.2	V
Differential time propagation delay, high to low	t_{PHLDT}	-	0.96	1.02	1.13	ns
Differential time propagation delay, low to high	t_{PLHDT}	-	0.94	0.98	1.09	ns
AC power current	I_{VDD25}	-	1.97	2.46	2.7	mA
Total AC power	W	-	4.93	6.15	6.75	mW
Clock jitter, rms	t_{RJ}	Without load	1.50	1.80	2.30	ps
Clock jitter, max (p-p)	t_{DJM}		2.04	2.27	2.90	ps
Data jitter, deterministic	t_{DJ}		12.4	12.7	13.7	ps
Input voltage high level	V_{IH}	For digital inputs	$0.8V_{DD25}$	-	V_{DD25}	V
Input voltage low level	V_{IL}		0	-	$0.2V_{DD25}$	V