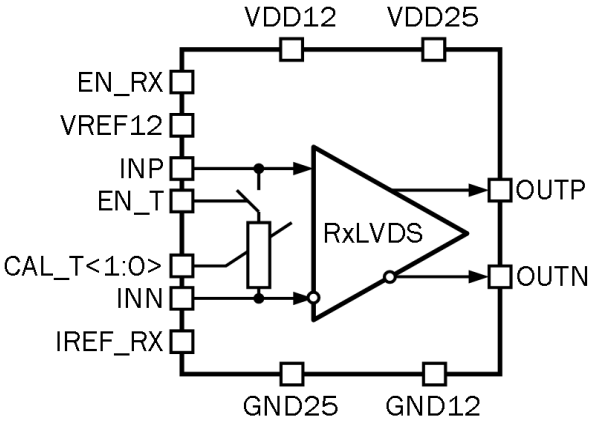
2 Gbps DDR rail to rail LVDS receiver

OVERVIEW

065TSMC_LVDS_10 is LVDS receiver with rail to rail input range. **EN_T** enables 100 Ohm internal resistor. The **CAL_T<1:0>** adjusts 100 Ohm internal resistor, the design target is to compensate the resistance deviation. The **VREF12** is input 1.2 V voltage reference. Pin **IREF_RX** to get current 20 uA reference from receiver bias. **INP** and **INN** are complementary input to connect to the bonding pads. This LVDS receiver does not employ hysteresis, and therefore does not comply with the hysteresis requirement of the TIA and IEEE standards for LVDS differential signaling at the specified rates.
IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 0.049mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply analog voltage	V_{DD25}	-		2.25	2.5	2.75	V
Supply digital voltage	V_{DD12}	-		1.08	1.2	1.32	V
Operating temperature range	T_j	-		-40	27	+85	°C
Input current range	I_{in}	EN_T= “1”		-	-	10	mA
Input common mode	V_{in}	-		0	1.2	2.4	V
Input differential threshold	V_{th}	-		-	-	100	mV
Receiver differential input impedance	R_{in}	With calibration		90	100	110	Ohm
		Without calibration T_CAL<1:0>= “10” or “01”		83	100	120	
		Without calibration T_CAL<1:0>= “11”		90	109	130	
DC current consumption	I_{DC}	@V_{DD25}		1.9	2.06	2.3	mA
Average current	I	F_{clk} = 1 GHz	@V_{DD25}	2.26	2.5	2.83	mA
			@V_{DD12}	78	89	103	uA
Stand-by current	I_{STB}	@V_{DD25}		12	21	98	nA
		@V_{DD12}		1	1.7	257	nA
Total average power	P_{TOTAL}	F_{clk} = 1 GHz		5.2	6.4	7.9	mW
Output voltage range	V_{out}	-		0	-	1.2	V
Differential propagation delay	t_{PHLDT}	High to low		453	587	872	ps
	t_{PLHDT}	Low to high		453	587	873	ps
Deterministic jitter, peak-to-peak	t_{DJ}	@2 Gbps		-	8.8	31	ps
		@1.8 Gbps		-	6.8	13.3	ps
		@1.6 Gbps		-	6.1	7.6	ps
Random jitter, rms	t_{RJ}	F_{clk}=1 GHz	$\|V_{INP} - V_{INN}\|$=100 mV	312	413	973	fs
			$\|V_{INP} - V_{INN}\|$=250 mV	154	194	388	
Random jitter, max (p-p)	t_{DJM}	F_{clk}=1 GHz	$\|V_{INP} - V_{INN}\|$=100 mV	4.4	5.8	13.6	ps
			$\|V_{INP} - V_{INN}\|$=250 mV	2.1	2.7	5.4	
Input voltage high level	V_{IH}	For digital inputs		0.8V_{DD12}	-	V_{DD12}	V
Input voltage low level	V_{IL}			0	-	0.2V_{DD12}	V