Programmable LVDS Transmitter/Receiver

SPECIFICATION

1 FEATURES

- TSMC 90nm CMOS LP
- 1V CMOS input logic signal
- Output current digital 3 bit adjustment (from 0.75mA to 6.5mA)
- 1.6 Gbps (DDR MODE) switching rates for transmitter
- Low power dissipation (1.4 mW) for receiver
- Low power dissipation (16.56 mW) for transmitter
- Conforms to TIA/EIA-644 LVDS standards
- Military temperature range: from -60 °C to + 125 °C
- Propagation delay 590ps for transmitter
- Propagation delay 500ps for receiver
- Internal current digital 3 bit adjustment (high inner current for high frequency, from 40 to 300uA) for receiver
- Portable to other technologies (upon request)

2 APPLICATION

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

3 OVERIVIEW

LVDS circuit consists of transmitter (LVDSOUT), receiver (LVDSIN) and bias. The LVDS transmitter consists of a current source (nominal 3.5 mA) that drives the differential pair lines and common-mode regulator that provides the output common-mode voltage signal equal 1.25V. The output current adjustment is defined by the digital code register ilvo<2:0>. The receiver has high DC input impedance (~MΩ), so the majority of driver current flows across the 100 Ω external termination resistor generating about 350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid “one” or “zero” logic state. That is it transforms input 350 mV signal to CMOS 1.8 V output signal. The internal current adjustment is defined by digital code register ilvi<2:0>.

4 STRUCTURE

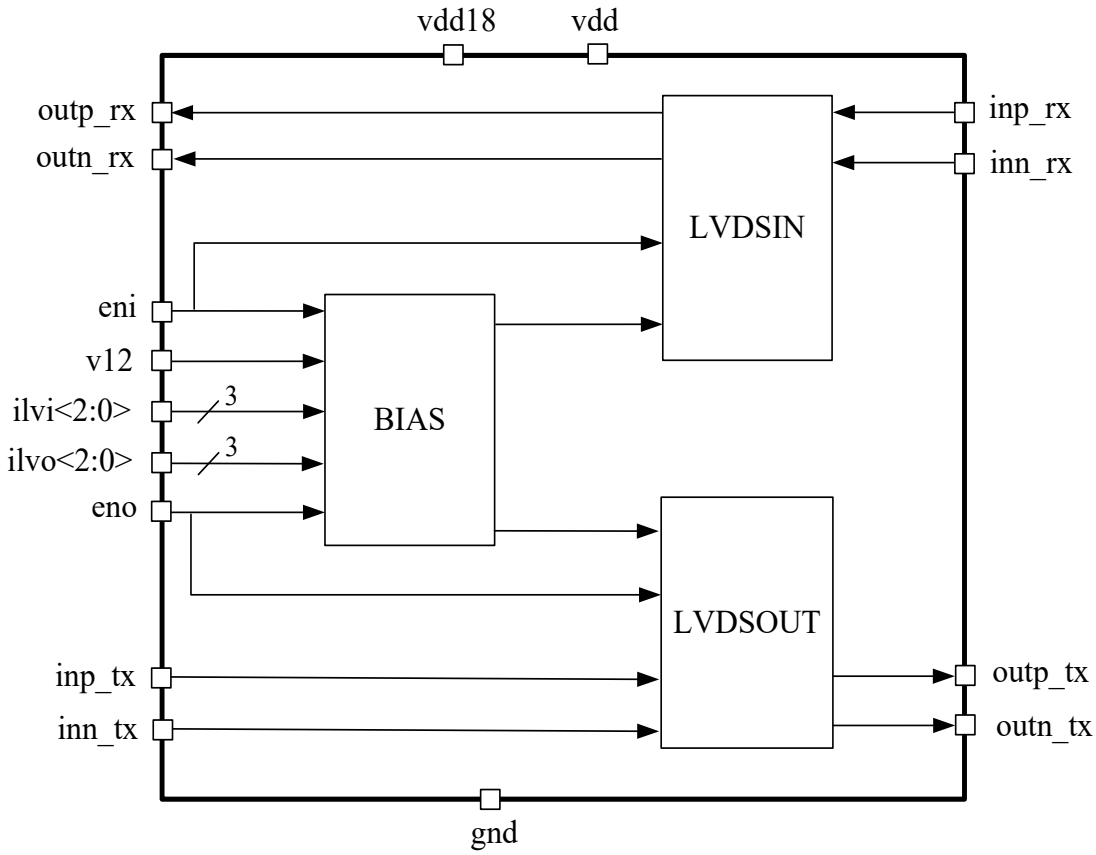

Figure 1: Programmable LVDS Transmitter/Receiver structure.

5 PIN DESCRIPTION

Name	Direction	Description
inp_tx inn_tx	I	Input differential CMOS 1V signal of transmitter
inp_rx inn_rx	I	Input differential LVDS signal of receiver
v12	I	Reference voltage 1.2V
ilvi<2:0>	I	Digital code of internal current adjustment of receiver
ilvo<2:0>	I	Digital code of output current adjustment of transmitter
eni	I	Enable/disable of receiver
eno	I	Enable/disable of transmitter
outp_rx outn_rx	O	Output differential CMOS 1.8V signal of receiver
outp_tx outn_tx	O	Output differential LVDS signal of transmitter
vdd	IO	Digital blocks supply voltage 1V
vdd18	IO	Analog blocks supply voltage 1.8V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Transmitter dimensions are given in the table 1, receiver dimensions are given in the table 2.

Table 1: Block dimensions of LVDS transmitter.

Dimension	Value	Unit
Height	45	µm
Width	57	µm

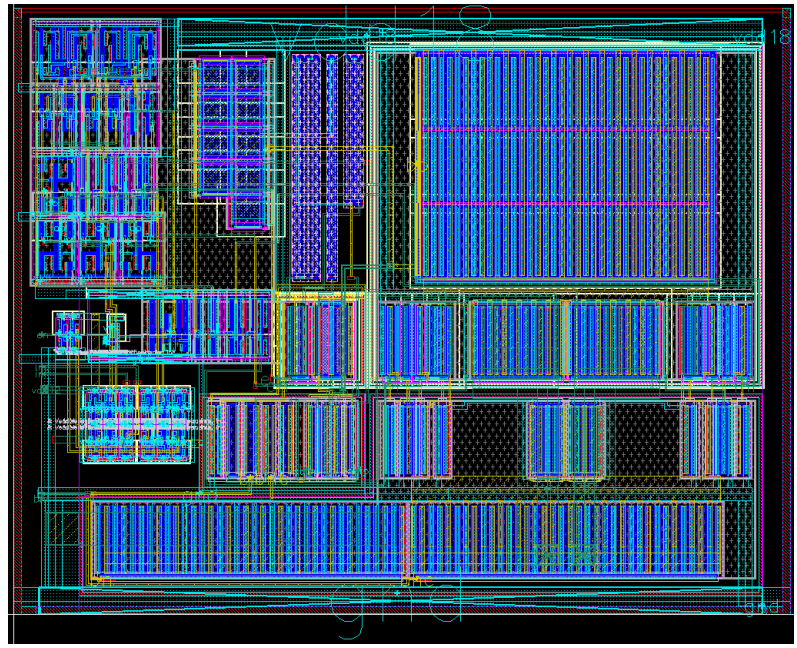

Figure 2: LVDS Transmitter layout view.

Table 2: Block dimensions of LVDS receiver.

Dimension	Value	Unit
Height	36	µm
Width	70	µm

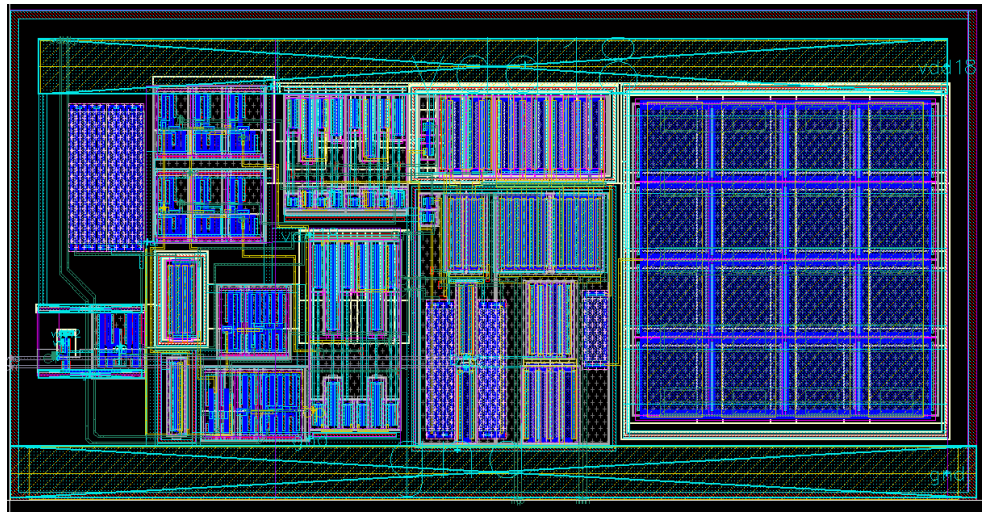

Figure 3: LVDS Receiver layout view.

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC 90nm CMOS Logic Process
Status silicon proven
Area 0.01 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd18} = 1.71 ÷ 1.89 V, V_{dd}= 0.95 ÷ 1.05 and T = -60 ÷ +125 °C. Typical value are at V_{dd18}= 1.8V, V_{dd}= 1V, T = + 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply analog voltage	V_{dd18}	-	1.71	1.8	1.89	V
Supply digital voltage	V_{dd}	-	0.95	1	1.05	V
Operating temperature range	T	-	-60	+27	+125	°C
Differential output voltage	V_{OD}	For transmitter	270	360	510	mV
Offset voltage	V_{OS}	For transmitter	1.18	1.25	1.31	V
Differential time propagation delay, high to low	t_{PHLDT}	For transmitter	330	427	573	ps
Differential time propagation delay, low to high	t_{PLHDT}	For transmitter	342	442	588	ps
Output rise time	t_{RT}	For transmitter	46	47	48	ps
Output fall time	t_{FT}	For transmitter	60	61	65	ps
Stand-by current	I_{st}	Total	-	190	-	nA
Differential time propagation delay, high to low	t_{PHLDR}	For receiver	271	308	497	ps
Differential time propagation delay, low to high	t_{PLHDR}	For receiver	276	347	501	ps
Low power dissipation	W_{tr}	For transmitter	-	-	16.56	mW
Low power dissipation	W_{rc}	For receiver	-	-	1.4	mW
Total low power dissipation	W_t	Receiver+transmitter	-	-	17.96	mW
Input voltage range	V_{in}	For transmitter	0	-	1	V
Output voltage range	V_{out}	For receiver	0	-	1.8	V
Change to V_{OS}	ΔV_{OS}	For transmitter	-	-	15	mV
Out current for transmitter	I_{out}	ilvo<2:0>=1.1.1	4.9	6.5	8.4	mA
Current consummation for transmitter	I_{ctr}	ilvo<2:0>=1.1.1	-	6.5	-	mA
Current consummation for receiver	I_{crc}	ilvi<2:0>=1.1.1	-	0.64	-	mA
High Level Input Voltage	V_{IH}	For digital inputs	0.7	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.3	V
Clock jitter, random rms	t_{RJ}	For transmitter C_L=3p	-	126	212	fs
Clock jitter, random max (p-p)	t_{DJM}		-	257	452	fs
Data jitter, deterministic	t_{DJ}		-	5.1	6.67	ps
Clock jitter, random rms	t_{RJ}	For transmitter C_L=0p	-	59	213	fs
Clock jitter, random max (p-p)	t_{DJM}		-	150	486	fs
Data jitter, deterministic	t_{DJ}		-	1.32	2.34	ps
Clock jitter, random rms	t_{RJ}	For receiver	-	0.79	0.95	ps
Clock jitter, random max (p-p)	t_{DJM}		-	1.16	1.5	ps
Data jitter, deterministic	t_{DJ}		-	17.2	21.4	ps

8 DELIVERIBLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
    - Table 7.2 (page 5)