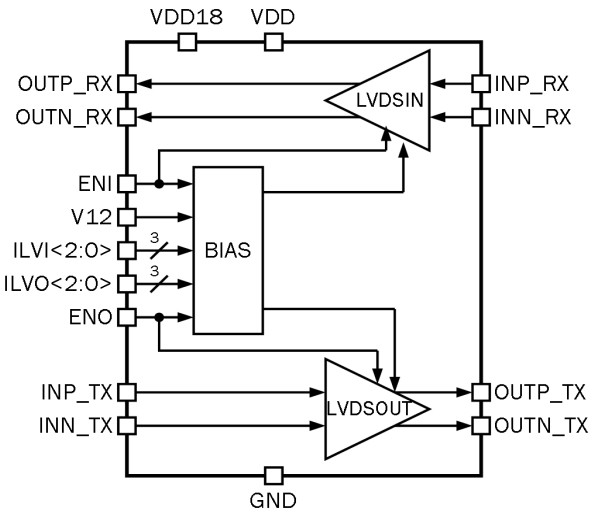
1.6 Gbps DDR Programmable LVDS transmitter/receiver

OVERVIEW

090TSMC_LVDS_02 consists of transmitter (LVDSOUT), receiver (LVDSIN) and a bias. The LVDS transmitter consists of a current source (nominal 3.5mA) that drives the differential pair lines and common-mode regulator, which provides the output common-mode voltage signal equal 1.25V. The output current adjustment is defined by the digital code register **ILVO<2:0>**. The receiver has high DC input impedance, so the majority of driver current flows across the 100Ohm external termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid logic state of "1" or "0". That is, it transforms 35mV input signal to CMOS 1.8V output signal. The internal current setting is defined by digital code register **ILVI<2:0>.**



IP technology: TSMC CMOS LP 90 nm.
IP status: silicon proven.
Area: 0.01mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				min	typ.	max	
Supply analog voltage	V_{DD18}	-		1.71	1.8	1.89	V
Supply digital voltage	V_{DD}	-		0.95	1	1.05	V
Operating temperature range	T_j	-		-60	+27	+125	°C
Differential output voltage	V_{OD}	For transmitter		270	360	510	mV
Offset voltage	V_{OS}	For transmitter		1.18	1.25	1.31	V
Output rise time	t_{RT}	For transmitter		46	47	48	ps
Output fall time	t_{FT}	For transmitter		60	61	65	ps
Stand-by current	I_{st}	Total		-	190	-	nA
Sampling rate	F_S	DDR mode		-	1.6	-	Gbps
Power dissipation	W_{tr}	For transmitter		-	-	16.56	mW
	W_{rc}	For receiver		-	-	1.4	mW
Total power dissipation	W_t	Receiver + transmitter		-	-	17.96	mW
Output voltage range	V_{out}	For receiver		0	-	1.8	V
Output current for transmitter	I_{out}	ILVO<2:0>=1.1.1		4.9	6.5	8.4	mA
Current consummation	I_{ctr}	ILVO<2:0>=1.1.1	For transmitter	-	6.5	-	mA
	I_{crc}	ILVI<2:0>=1.1.1	For receiver	-	0.64	-	mA
Input logic-level high	V_{IH}	For digital inputs		0.7	-	-	V
Input logic-level low	V_{IL}			-	-	0.3	V
Clock jitter, random rms	t_{RJ}	For transmitter C_L=3pF		-	126	212	fs
Clock jitter, random max (p-p)	t_{DJM}			-	257	452	fs
Data jitter, deterministic	t_{DJ}			-	5.1	6.67	ps
Clock jitter, random rms	t_{RJ}	For transmitter		-	59	213	fs
Clock jitter, random max (p-p)	t_{DJM}			-	150	486	fs
Data jitter, deterministic	t_{DJ}			-	1.32	2.34	ps
Clock jitter, random rms	t_{RJ}	For receiver		-	0.79	0.95	ps
Clock jitter, random max (p-p)	t_{DJM}			-	1.16	1.5	ps
Data jitter, deterministic	t_{DJ}			-	17.2	21.4	ps