Up to 400 Mbps DDR LVDS receiver

OVERVIEW

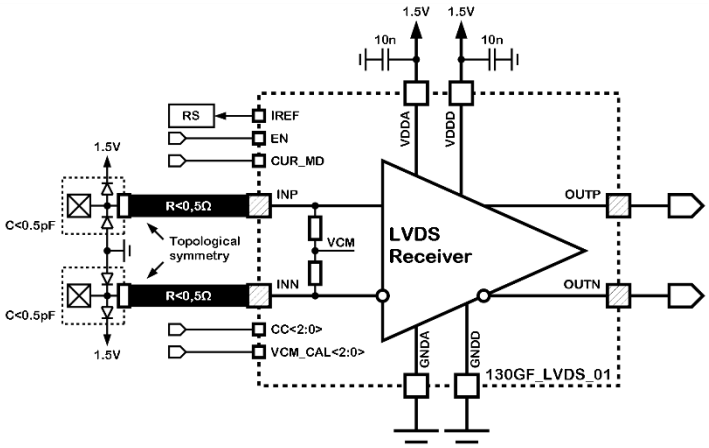
130GF_LVDS_01 is a LVDS receiver with data rate up to 400 Mbps (DDR mode). The LVDS receiver converts input LVDS signal to differential CMOS 1.5V standard and transmits it through the OUTP and OUTN outputs. The input signal can be supplied with or without AC decoupling. If the signal is supplied to the receiver input without AC decoupling, then it must have an external VCM. Otherwise, the internal VCM is used. The IP block can be used as a clock receiver with frequency up to 1.2 GHz. The LVDS has a terminating resistor with an adjustable value. The internal reference current can be adjusted to optimize the power consumption of the LVDS receiver.

Features:

- TIA/EIA-644 LVDS standards without hysteresis
- Data transfer rate: up to 400 Mbps (DDR mode)
- Clock frequency: up to 1.2 GHz
- VDDA voltage supply for analog part
- VDDD voltage supply for digital part
- 1.5V CMOS logic level
- Area: 98×81 um^2
- Global Foundries 130 nm CMOS technology

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	VDDD	For digital part	1.425	1.5	1.575	V
	VDDA	For analog part	1.425	1.5	1.575	
Operating temperature range	T_j	-	-40	+27	+125	°C
Reference current	I_{REF}	-	-	10	-	uA
Common-mode input voltage	VCM_{IN}	@external common-mode	0.875	-	VDDA–0.15	V
		@internal common-mode	-	1.2	-	
Clock frequency	F_{CLK}	-	-	-	1.2	GHz
Data transfer rate	F_S	DDR mode	-	-	400	Mbps
Input differential threshold	V_{th_in}	-	-	-	100	mV
Input impedance of internal terminator	Z_{in}	-	90	100	110	Ω
Clock signal duty cycle	S	-	-	50	-	%
Clock jitter, rms	τ	-	-	46	-	ps
Total current consumption	IDD	@F_S = 400MBPS	-	2.0	-	mA
		@F_{CLK} = 1GHz	-	2.5	-	
	I_{shtd}	Shutdown mode	-	-	171	nA