Up to 1.25 Gbps DDR LVDS IPs library

OVERVIEW

130TSMC_LVDS_04 is a library including:

- Transmitter LVDS driver (LVDS_TX);
- Receiver LVDS driver (LVDS_RX);
- Bandgap reference block (LVDS_BG);
- Bias blocks (LVDS_BIASRXnX, LVDS_BIASTXnX) for receiver and transmitter with the number of output currents (n = 1, 2, 4, 8, 16, 32)

The bias blocks LVDS_BIASRXnX is intended to generate output currents for LVDS_RX drivers and LVDS_BIASTXnX could generate output currents for LVDS_RX and LVDS_TX drivers both. LVDS_RX cells comprise a voltage comparator with input connected to the 100Ohm termination resistor by **EN_RES** pin.

IP technology: TSMC CMOS 130nm.

IP status: pre-silicon verification.

Area: LVDS_TX driver – 0.023mm^2;
LVDS_RX driver – 0.034mm^2;
LVDS_RXTX driver – 0.057mm^2;
LVDS_BG – 0.044mm^2;
LVDS_BIASRX1X – 0.034mm^2;
LVDS_BIASRX32X – 0.052mm^2;
LVDS_BIASTX1X – 0.035mm^2;
LVDS_BIASTX32X – 0.054mm^2.

Features:

- 3.3V IO power supply
- 1.2V Core power supply
- 1.2V CMOS input and output logic signals
- LVDS_BIASTXnX adjustable output current (range from 0.75mA to 6.5mA)
- LVDS_BIASRXnX adjustable output current (range from 6.25uA to 37.5uA)
- 1.25 Gbps (DDR MODE) switching rates
- TIA/EIA-644 LVDS standards without hysteresis
- Two receiver cell types: rail to rail and reduced input range
- 1.2V/3.3V level shifters
- TSMC 130nm CMOS technology

Applications:

- Point-to-point data transmission
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data transmission
- Cable data transmission

BLOCK DIAGRAM

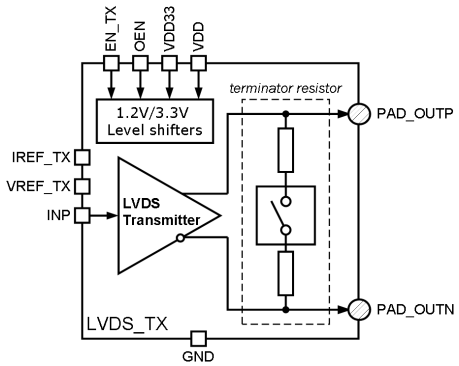

Figure 1: **LVDS_TX** driver block diagram

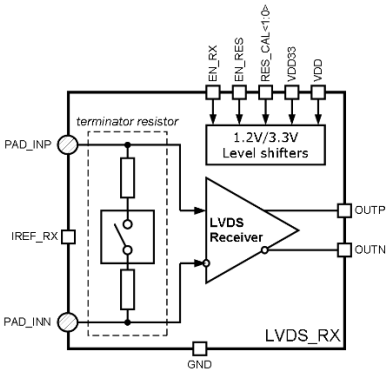

Figure 2: **LVDS_RX** driver block diagram

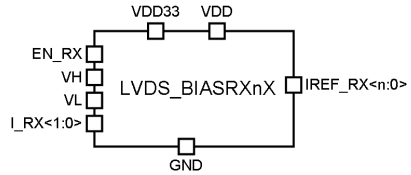

Figure 3: **LVDS_BIASRXnX** block diagram

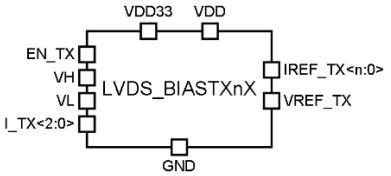

Figure 4: **LVDS_BIASTXnX** block diagram

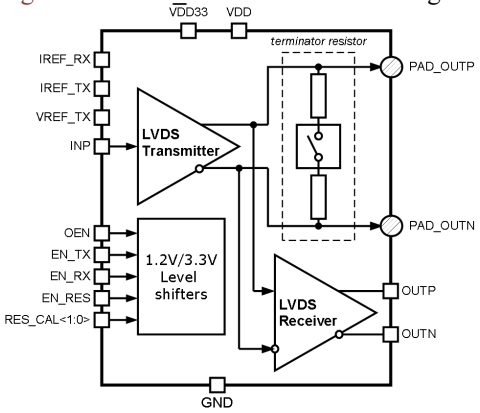

Figure 5: **LVDS_RXTX** block diagram

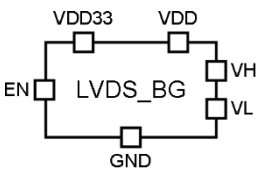

Figure 6: **LVDS_BG** block diagram