1Gbps Rail to Rail LVDS receiver

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.13 um
- 3.3 V power supply
- 1 Gbps (DDR MODE) switching rates
- Conforms to TIA/EIA-644 LVDS standards without hysteresis
- Rail to rail input range
- Temperature range: -40 °C to + 85 °C
- Optimized for pad-limited layout design
- Portable to other technologies (upon request)

2 APPLICATION

- Point-to-point data receiver
- Multidrop buses
- Clock distribution
- Backplane receiver
- Backplane data receiver
- Cable data receiver

3 OVERVIEW

The LVDS receiver converts LVDS data to CMOS data stream. It could receive data or clock signals with rate up to 1Gbps DDR MODE. The LVDS receiver has rail to rail input range and corresponds to TIA/EIA-644 LVDS standards without hysteresis. There is also embedded terminator which can be enabled/disabled by the control pin (EN_RES).
The LVDS receiver is designed on TSMC SiGe BiCMOS 0.13 um technology.

4 STRUCTURE

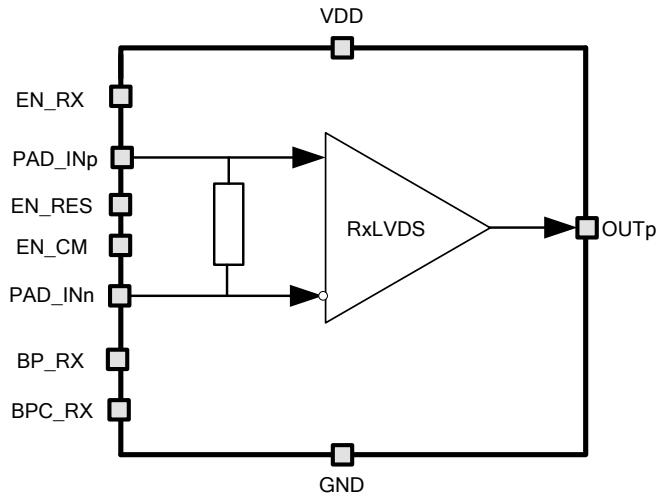

Figure 1: Rail to rail LVDS receiver 1 Gbps structure.

5 PIN DESCRIPTION

Name	Direction	Description
EN_CM	I	Input common-mode voltage enable
EN_RES	I	On-chip resistor enable
EN_RX	I	LVDS receiver enable
PAD_INp	I	Input differential LVDS signal
PAD_INn		
OUTp	O	Output CMOS signal
BP_RX	I	Voltage reference from bias
BPC_RX		
VDD	IO	Supply voltage 3.3 V
GND	IO	Ground

Table 1: LVDS receiver truth table.

Mode	Input			Output
	EN_RX	PAD_INp	PAD_INn	OUTp
Receive	1	1	0	1
		0	1	0
Power down	0	X	X	0

6 LAYOUT DESCRIPTION

Rail to Rail LVDS Receiver dimensions are given in the table 2.

Table 2: Block dimension.

Dimension	Value	Unit
Height	170	um
Width	140	um

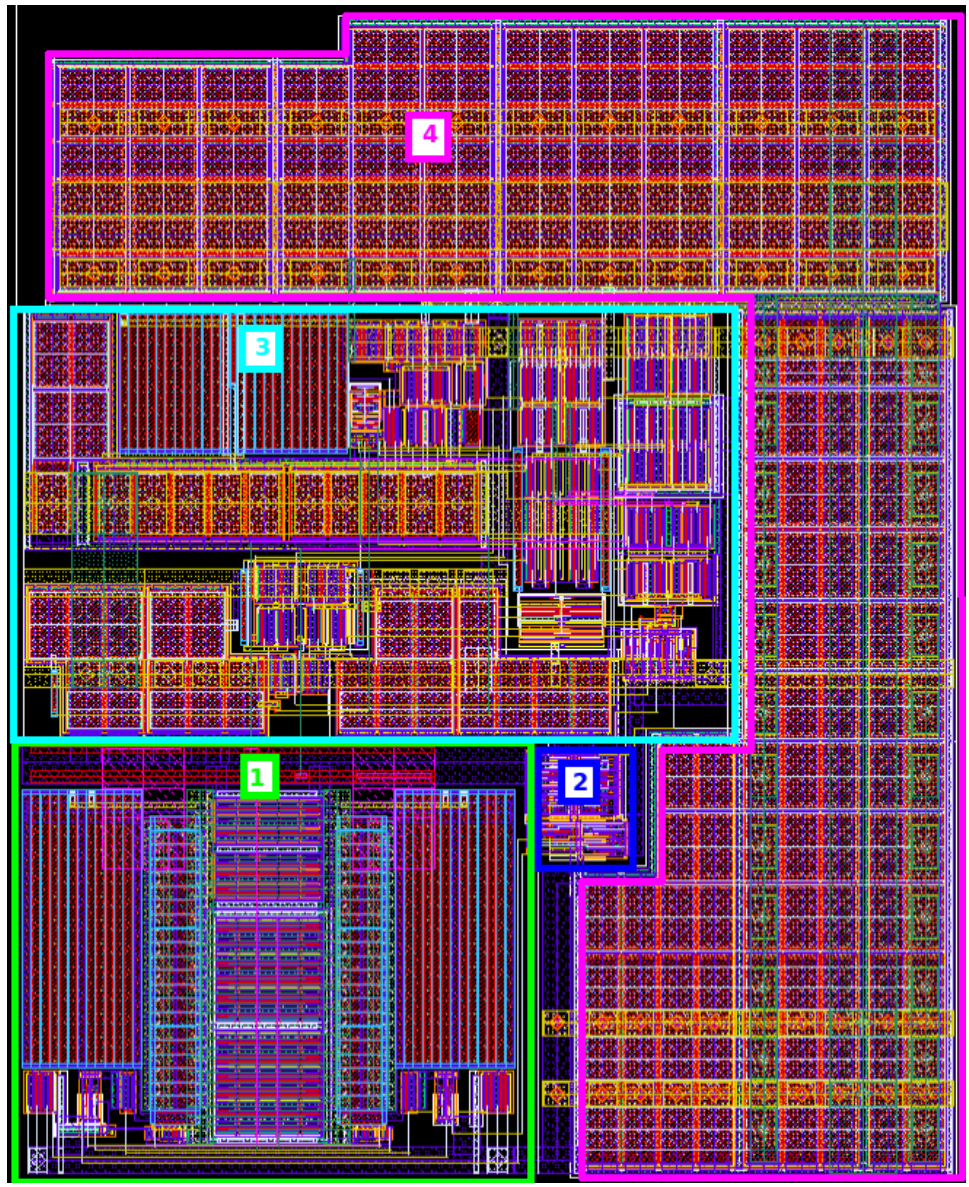

Figure 2: Rail to rail LVDS Receiver layout view.

1. On-chip 100 ohm resistor
2. Digital buffer
3. Rail to rail LVDS receiver
4. MOS capacitors

7 OPERATING CHARACTERISRICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SiGe BiCMOS 0.13um
Status _____ pre-silicon verification
Area _____ 0.023 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are special for V_{dd} = 2.7 ÷ 3.6 V, T = -40 ÷+85 °C. Typical value are at V_{dd}= 3.3V, T=+ 85 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply analog voltage	V_{dd}	-	2.7	3.3	3.6	V
Operating temperature range	T	-	-40	27	+85	°C
Input voltage range (common-mode)	V_{in}	-	0	1.2	3.3	V
Input differential threshold	V_{th}	-	-		100	mV
Receiver differential input impedance	R_{in}	-	90	107	130	Ω
DC power current from V_{dd}	I_{VDD}	-	0.89	0.97	1.1	mA
Total DC power	W	-	2.4	3.2	3.96	mW
Stand-by current	I_{st}	-	1	1.5	11	nA
Output voltage range	V_{out}	-	0	-	3.3	V
Differential time propagation delay, high to low	t_{PHLDT}	-	0.77	1.1	1.7	ns
Differential time propagation delay, low to high	t_{PLHDT}	-	0.77	1.1	1.7	ns
AC power current from V_{dd}	I_{VDD}	-	1.25	1.47	1.66	mA
Total AC power	W	-	3.4	4.85	6	mW
Clock jitter, rms	t_{RJ}	C_L=100f	1.1	1.9	2.4	ps
Clock jitter, max (p-p)	t_{DJM}		5.4	10.8	12	ps
Data jitter, deterministic	t_{DJ}		2.7	11	17	ps
Input voltage high level	V_{IH}	For digital inputs	0.8 V_{dd}	-	V_{dd}	V
Input voltage low level	V_{IL}		0	-	0.2 V_{dd}	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 1
- Section 3
- Subsection 7.2 update