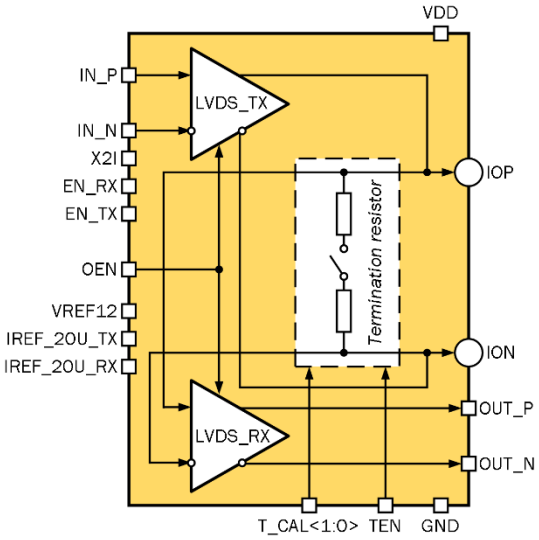
1.2 Gbps DDR LVDS transmitter/receiver

OVERVIEW



180TSMC_LVDS_09 core logic interface in receiver part includes complementary signal pins (**OUT_P** and **OUT_N**) for data transmission and control pins for receiver configuration. Core logic interface in transmitter part includes complementary signal pins (**IN_P** and **IN_N**) for data transmission and control pins for transmitter configuration. Internal analog pins **VREF12**, **IREF_20U_TX**, **IREF_20U_RX** are reference voltage and currents inputs. Bi-directional differential pins **IOP** and **ION** should be connected to bonding pads. The block may operate as LVDS receiver, transmitter or half-duplex transceiver. The latter one is selected by setting both **EN_TX** and **EN_RX** controls to "1". In this case port direction is toggled by **OEN** control ("1" - RX, "0" - TX). In RX mode transmitter output is switched to high-impedance state, while in TX mode internal termination is disabled. In single-direction applications configuration should be selected by **EN_TX**, **EN_RX** pins in order to save power. Double output current option (**X2I** = "1") is included for dual termination designs – near-end and far-end. Internal termination is switched on by **TEN** control and its value may be calibrated from 20% to 10% deviation using **T_CAL<1:0>** parameter.

IP technology: TSMC 180nm CMOS.

IP status: pre-silicon verification.

Area: 0.06mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				min	typ.	max	
Analog supply voltage	V_{DD}	-		3.0	3.3	3.6	V
Operating temperature range	Tj	-		-60	+27	+100	°C
Differential output voltage	V_{OD}	$\|V_{IOP}- V_{ION}\|$, transmitter mode	X2I = "0"	300	320	340	mV
			X2I = "1"	305	320	335	mV
Output offset voltage	V_{OS}	$\|V_{OS}\|=\| V_{IOP} + V_{ION} \| /2$		1.88	1.2	1.22	V
Data rate	F_S	DDR mode		-	1.2	-	Gbps
Rise time	t_{RT}	20% to 80%, transmitter mode, C_{LTX} = 1pF		132	134	154	ps
Fall time	t_{FT}			131	133	153	ps
Differential time propagation delay	t_{PHL}	Transmitter mode, C_{LTX} = 1pF	High to low	0.92	1.29	2.1	ns
	t_{PLH}		Low to high	0.92	1.29	2.1	ns
Total AC power	W_{AC}	Transmitter mode, EN_RX="0", F_s=600MHz		16.5	19.8	23	mW
Clock jitter, rms	t_{RJ}			256	375	665	fs
Data jitter, deterministic	t_{DJ}			0.3	1.9	3.2	ps
Input voltage range (common-mode)	V_{in}	Receiving mode		0	-	2.4	V
Input differential threshold	V_{th}			-	-	100	mV
Input impedance	Z_{in}	-		90	100	110	Ohm
Differential time propagation delay	t_{PHL}	Receiving mode, C_L=50fF, V_{ind}=100mV	High to low	0.69	0.9	1.6	ns
	t_{PLH}		Low to high	0.69	0.9	1.6	ns
Clock signal duty cycle	S	Receiving mode, F_s=620MHz		46	50	54	%
Total AC power	W_{AC}	Receiving mode, EN_TX="0", F_s=600MHz		6.3	7.6	9.3	mW
Clock jitter, rms	t_{RJ}	Receiving mode, C_L=50fF, V_{ind}=100mV		0.59	0.85	3.3	ps
Data jitter, deterministic	t_{DJ}			2	4	80	ps
OEN to output enable (V_{OS})[1]	T_{OE}	Transmitter		5	7	10	ns
OEN to output disable (V_{OS})[2]	T_{OD}			1.5	2	2.5	ns
Stand-by current	I_{st}	-		0.9	1	12.5	nA

Notes: [1] Output recovery to voltage within the offset voltage range;
[2] Output drops out of the output offset voltage range.