1571.3 to 1606.4 MHz mixer with polyphase filters

SPECIFICATION

1 FEATURES

- SMIC CMOS 0.18 µm
- Adjusted gain
- Built-in matched input
- Reference current 10 µA
- Supply voltage 1.8 V
- Temperature compensation
- Adding of built-in 1.8 V voltage regulator available
- Portable to other technologies (upon request)

2 APPLICATION

- Mobile devices
- Navigation receiver

3 OVERVIEW

The cell includes matched input, intermediate and output buffers with gain control, separated quadrature mixers and polyphase filter. Quadrature mixer is based on Gilbert cells and converts RF frequency to a low intermediate frequency (IF). Polyphase filter is used to block image frequency signal. Buffer amplifiers are used to improve qualitative characteristics, reduce input signals and improve output signals, reduce rejection, harmonic and intermodulation distortions. The block is fabricated on SMIC CMOS 0.18µm technology.

4 STRUCTURE

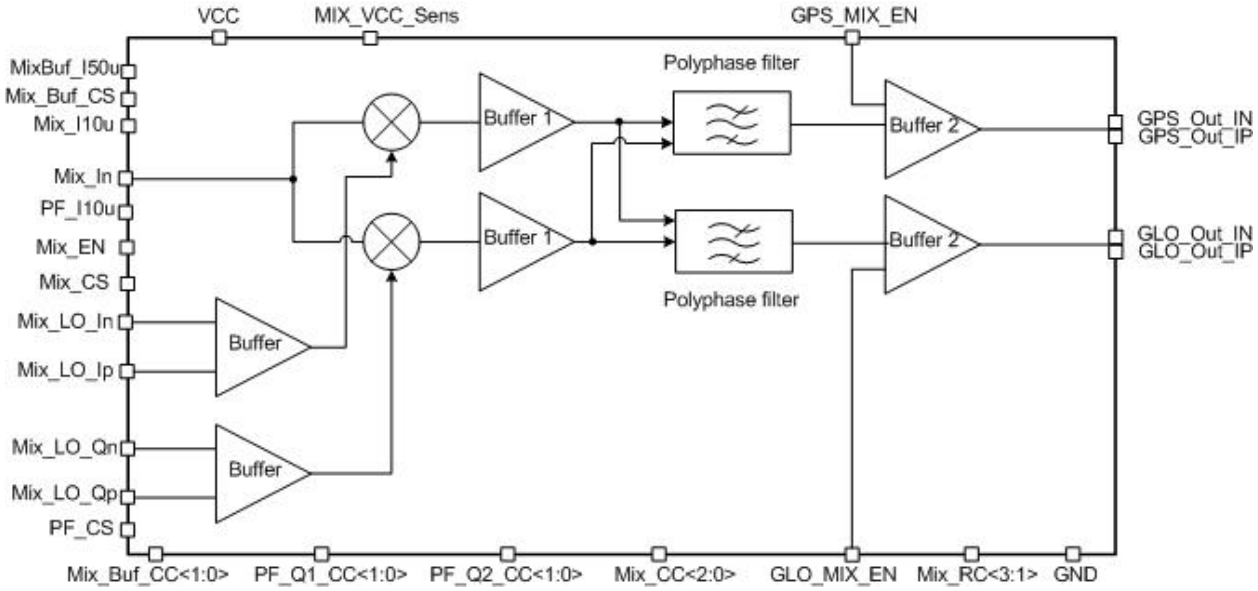

Figure 1: Mixer structure

5 PIN DESCRIPTION

Name	Direction	Description
MixBuf_I50u	I	Buffer reference current (50 µA)
Mix_I10u	I	Mixer reference current (10 µA)
Mix_In	I	Mixer differential input
PF_I10u	I	Polyphase filter buffer current
Mix_EN	I	Enable/disable
GLO_MIX_EN	I	Mixer channel 1 enable/disable
GPS_MIX_EN	I	Mixer channel 2 channel enable/disable
Mix_CS	I	Mixer temperature compensation mode enable
MIX_LO_In	I	Quadrature mixer differential input for local-oscillator signals
MIX_LO_Ip	I	
MIX_LO_Qn	I	
MIX_LO_Qp	I	
GLO_Out_IP	O	Mixer channel 1 differential output
GLO_Out_IN	O	
GPS_Out_IP	O	Mixer channel 2 differential output
GPS_Out_IN	O	
PF_CS	I	Polyphase filter temperature compensation mode enable
Mix_Buf_CC<1:0>	I	Buffer current consumption control
PF_Q1_CC<1:0>	I	Buffer 1 current consumption control
PF_Q2_CC<1:0>	I	Buffer 2 current consumption control
MIX_CC<2:0>	I	Mixer current consumption control
MIX_RC<2:0>	I	Input matching adjustment
MIX_VCC_Sens	IO	Power indicator
VCC	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	964.26	µm
Width	898.92	µm

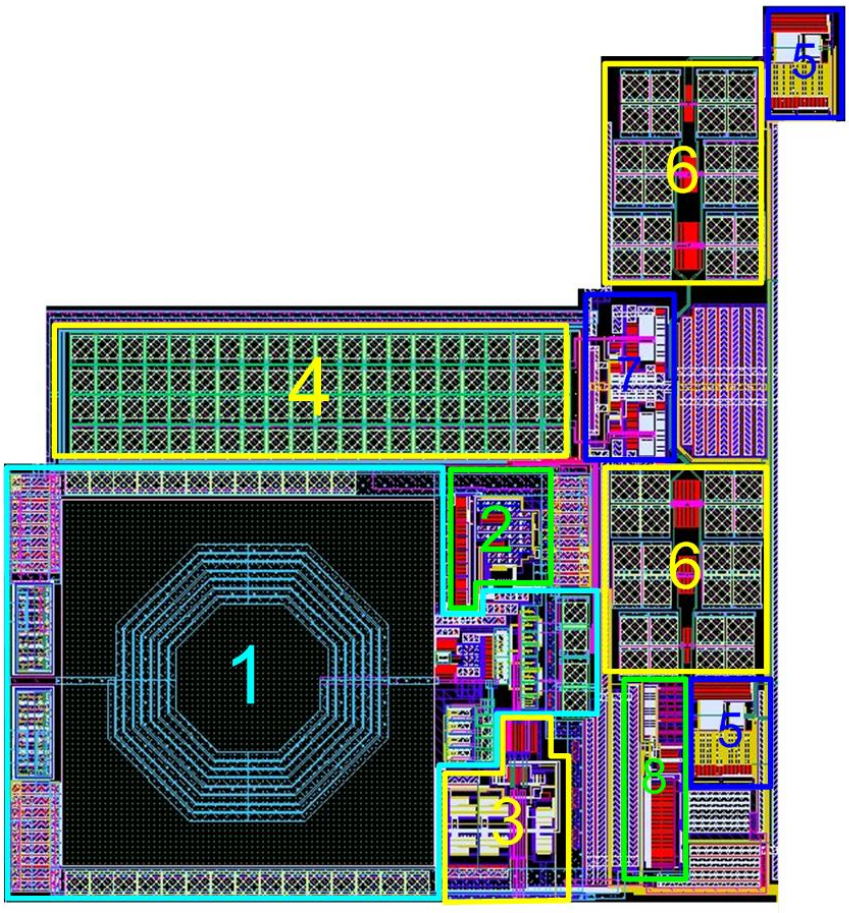

Figure 2: Device layout

1. Mixer core
2. Reference current source
3. Mixer buffer
4. Separating capacitors
5. Polyphase filter output buffer
6. Polyphase filter
7. Polyphase filter input buffer
8. Polyphase filter reference current

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology SMIC CMOS 0.18 µm
Status silicon proven
Area 0.6 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.7 ÷ 1.9 V and T = -45 ÷ +90 °C. Typical values are at V_{cc} = 1.8 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.7	1.8	1.9	V
Operating temperature range	T	-	-45	27	90	ºC
Input frequency range	F_{in}	-	1571.3	-	1606.4	MHz
Local-oscillator frequency	F_{osc}	-	-	1589.8	-	MHz
Output frequency range	F_{out}	-	7.3	-	18.4	MHz
Input SWR	SWR	50 Ω without external matching circuits	-	1.3	1.4	-
Noise figure	NF	-	-	9.4	10	dB
Power gain	Gp	Signal source 50 Ω, loading 2 kΩ	-	5.4	-	dB
Gain ripple	G	-	-	-	2.0	dB
Input 1dB compression point	P_{1dB}	-	-	-33	-	dBm
Input impedance	R_{in}	-	1800	2000	2200	Ω
Peak-to-peak voltage at mixer differential input	A	With loading 1pF	-	1.280	-	mV
Polyphase filter poles	P_S	-	-	4.8	-	MHz
			-	10.0	-	
			-	21.0	-	
Image channel rejection	S_{ch}	At quadrature signals differed from 90º no more than 3º	35.15	-	-	dB
Group delay time ripple	t_{del}	In IF range in view of polyphase filter	-	7.81	-	ns
Current consumption	I_{cc}	-	-	4.95	-	mA
Current consumption in a standby mode	I_{stb}	-	-	12.96	-	nA
Input logic-high level	V_{IH}	For digital inputs	0.7 V_{cc}	-	3.6	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Note:
The local-oscillator with rectangular pulse is recommended to use for getting optimal parameters.

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation