13.56MHz NFC Transceiver IP

SPECIFICATION

1 FEATURES

- TSMC 40nm CMOS EMBEDDED Memory FLASH RF ULP
- Operating temperature range –40…+85 °C
- Battery voltage support from 2.3V to 5.5V
- IO dedicated voltage from 1.62 to 3.3V
- Interfaces
  - I2C-bus: fastmode, fastmode plus and high-speed modes with data rate of 3.4MBd/s
  - SPI-bus: support master and slave mode, clock frequency of 20MHz
  - UART-bus: 300-115200bps
  - 3 SWP interfaces
- Integrated DCDC booster: support input supply 2.3V to 4.8V
- Support 3 UICC
- Support Class B and C operating conditions for UICC
- ARM Cortex-M0+ core (or RV32IMC or RV32GC)
  - Flash: 256KB
  - RAM: 20KB
  - ROM: 64KB
  - CPU clock: 100MHz
- ISO/IEC 14443A/B PICC mode (106/212/424/848kbps) compliant with EMVCo PICC and NFC Forum
- ISO/IEC 14443A/B PCD mode (106/212/424/848kbps) designed according to NFC Forum digital protocol T4T platform and ISO-DEP
- FeliCa PICC/PCD mode (212/424kbps)
- P2P mode (106/212/424kbps)
- ISO/IEC 15693 PCD mode
- NFC Forum PCD and tags T1T, T2T, T3T, T4T
- EMVCo PCD mode
- Standards compliance
  - NFC Forum Device Requirements
  - EMVCo for PICC and for PCD mode
  - ETSI/SCP 102 613 and 102 622 for SWP/HCI
- 3 different clock sources that can used as input to the NFC Contactless interface subsystem
- 27.12MHz quartz oscillator connected to XTAL1 and XTAL2
- External clock source (19.2/25/26/32/38.4/48MHz)
- 13.56MHz clock from internal VCO coming from the integrated PLL generates the 13.56MHz clock from 13.56MHz RF clock recovered from RF field
- Power consumption characteristics:
  - Power Off Mode 4uA
  - Standby Mode (support auto wake-up via RF field, internal timer, host I2C-bus interface, SWP) 38uA
  - Low Polling loop (Vbat =3.6V, T=25°C, loop time 500ms) 100uA
- RF characteristics
  - Card mode receiver sensitivity: down to 10mVpp
  - Reader mode receiver sensitivity: down to 0.3mVrms

- 2.5W output transmitter power

2 APPLICATION

- Mobile devices
- Portable equipment
- Consumer devices
- Wearable devices

3 OVERVIEW

The IP is NFC Transceiver AFE which includes microcontroller and memories integration, power management unit, clock management unit, peripheral interfaces, analog frontend.
In addition, implemented first stage bootloader firmware (stored in ROM) which initializes minimal necessary parts of the system and loads actual firmware from Flash memory.
The IP contains ALM block, performs modulation by actively transmitting signal of an inversed polarity to suppress reader's signal thus enlarging AM depth. Long ALM sequences have recovered clock between the modulation pulses, so it can remain locked thus enriching tag emulation distance range.
In case implemented IP connection is done via NFC Controller Interface (NCI, software defined in NFC Forum). NCI is mapped to one of physical interfaces (I2C, SPI, UART).

4 FUNCTIONAL BLOCK DIAGRAM

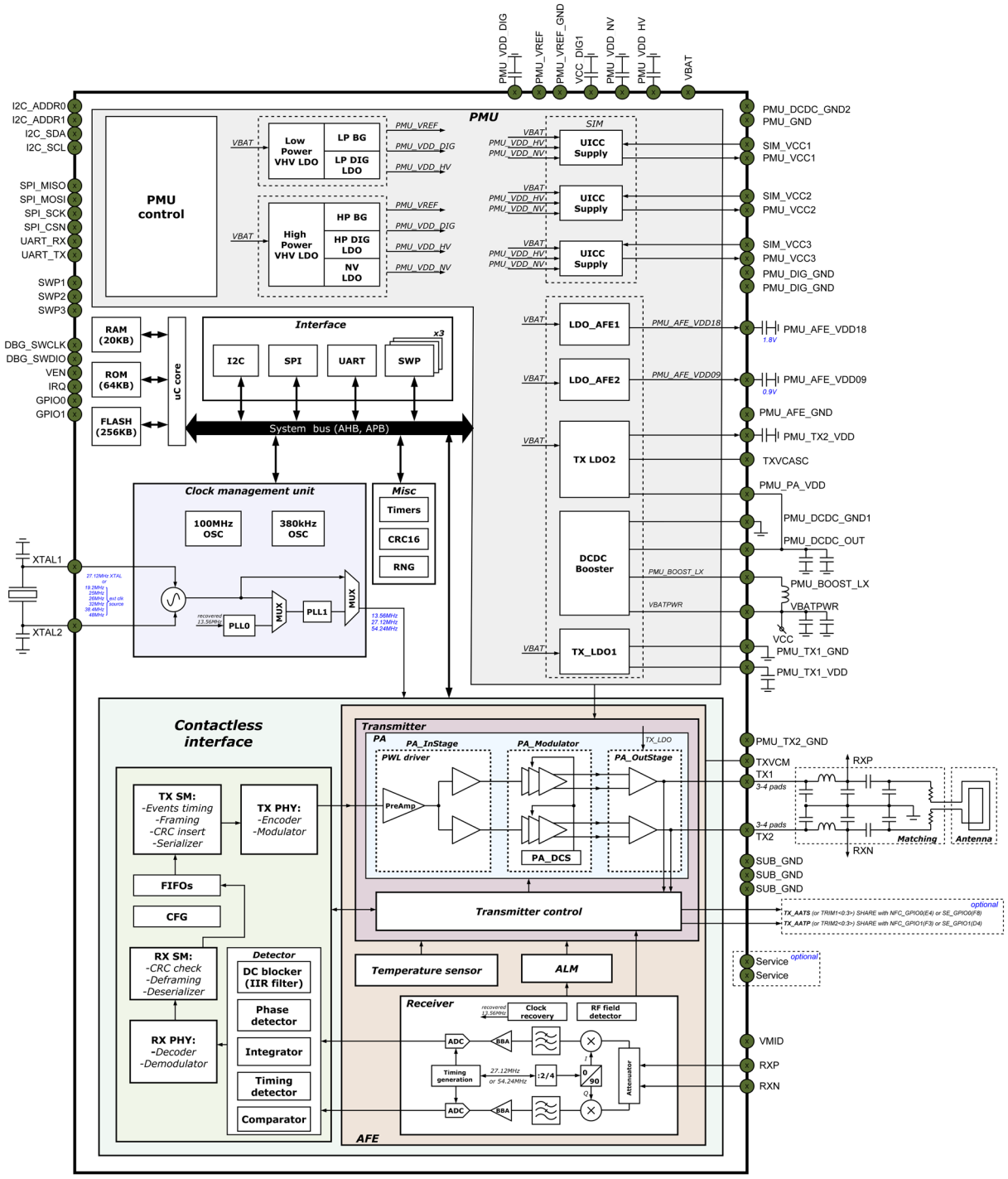

Figure 1: NFC Transceiver IP block diagram

5 PIN DESCRIPTION

Pin name	Direction	Voltage domain	Description
Power Management Unit			
VBAT	P	2.4-4.8V	Power Supply from Battery
VBATPWR	P	2.3-5.5V	Power Supply from Battery for DCDC
PMU_DCDC_GND1	G	-	DCDC GND pin
PMU_DCDC_GND2	G	-	DCDC GND pin
PMU_GND	G	-	PMU GND pin
PMU_VREF	O	-	Output reference voltage
PMU_VREF _GND	G	-	Ground connection for reference voltage
PMU_VDD_HV	P	1.8V	Power Supply for UICC (the output internal preregulator)
PMU_VDD_NV	P	1.8V	Power Supply for UICC (non-volatile memory supply)
PMU_AFE_VDD18	P	1.8V	Power Supply for PLL
PMU_AFE_VDD09	P	0.9V	Power Supply for NFC controller
PMU_AFE_GND	G		Ground connection for RF PLL
PMU_DCDC_OUT	O	5.5V	DCDC output voltage
PMU_VCC1	P	-	Power supply for SIM 1; to be connected to the ground if UICC interface is not used
SIM_VCC1	P	1.8V/3V	Power supply output to the SIM1
PMU_VCC2	P	-	Power supply for SIM 2; to be connected to the ground if UICC interface is not used
SIM_VCC2	P	1.8V/3V	Power supply output to the SIM2
PMU_VCC3	P	-	Power supply for SIM 3; to be connected to the ground if UICC interface is not used
SIM_VCC3	P	1.8V/3V	Power supply output to the SIM3
PMU_BOOST_LX	P	-	BOOST freq pin
PMU_VDD_DIG	P	0.9V	Internal generated common power supply for SN100T digital cores
PMU_DIG_GND	G	-	Ground connection to the digital domain
PMU_DIG_GND	G	-	Ground connection to the digital domain
PMU_PA_VDD	I	3.1-6V	Power supply for PA LDO
TXVCASC	P	0-5.5V	TX decoupling cap of the Low noise regulator
PMU_TX1_VDD	P	3.3V	Power supply for Transmitter control (TX_LDO1)
PMU_TX1_GND	G	N/A	Ground connection of the power amplifier (PA_InStage, PPA_Modulator)
PMU_TX2_VDD	P	1.5-5.7V	Power supply for power amplifier (PA_OutStage -> TX_LDO2)
PMU_TX2_GND	G	N/A	Ground connection of the power amplifier (PA_OutStage)
-	P	1.8V	Direct 1.8V input power for VDDC LD
IO_VDD	P	-	Power Supply for digital interface pads
Power Amplifier			
TXVCM	P	VDDPA	TX Voltage Common Mode
TX1	O	5.5V	Antenna driver output1
TX2	O	5.5V	Antenna driver output2
SUB_GND	G	N/A	ESD substrate ground connection
SUB_GND	G	N/A	ESD substrate ground connection
SUB_GND	G	N/A	ESD substrate ground connection
Service	-	-	Internally connected; connect to ground
Service	-	-	Internally connected; leave open
Digital			
I2C_SDA	IO	VDD_IO	I2C interface data line
I2C_SCL	IO	VDD_IO	I2C interface synchronization line
I2C_ADDR0	I	VDD_IO	I2C interface address setup
I2C_ADDR1	I	VDD_IO	I2C interface address setup
SPI_MISO	IO	VDD_IO	SPI master/slave data line
SPI_MOSI	IO	VDD_IO	SPI master/slave data line
SPI_SCK	IO	VDD_IO	SPI master/slave clock

Pin name	Direction	Voltage domain	Description
SPI_CSN	IO	VDD_IO	SPI master/slave chip select
UART_RX	I	VDD_IO	Universal asynchronous receiver/transmitter input
UART_TX	O	VDD_IO	Universal asynchronous receiver/transmitter output
SWP1	IO	-	Single wire protocol 1 interface
SWP2	IO	-	Single wire protocol 2 interface
SWP3	IO	-	Single wire protocol 3 interface
DBG_SWCLK	I	?	Serial Wire Debug - clock input
DBG_SWDIO	IO	?	Serial Wire Debug - data input/output
VEN	I	-	Reset pin. Sets device in hard powerdown (OFF-Plus mode)
IRQ	O	-	Interrupt request output
GPIO0	IO	-	General purpose input/output
GPIO1	IO	-	General purpose input/output
Clock Management Unit			
XTAL1	I	-	PLL input1 clock (connected to crystal or system clock)
XTAL2	O	-	Crystal input2 (connected to crystal)
RX			
RXP	I	-	Positive receiver input
RXN	I	-	Negative receiver input
VMID	O	-	RX common mode voltage, which has to be connected to a de-coupling cap

Note: I – input, O – output, IO – input/output, P – power

This is not a final pinout and may be subject to change during the design stage.

6 LAYOUT DESCRIPTION

6.1 TECHNOLOGY OPTIONS

NFC Transceiver IP is designing under TSMC 40nm CMOS EMBEDDED Memory FLASH RF ULP technology process.

6.2 PHYSICAL DIMENSIONS

Current area estimation gives **7mm2**. Below is area estimation summary:

- TX path 0.66 mm2
- RX path 2.46 mm2
- CMU 0.52 mm2
- PMU 2.25 mm2
- Digital 1.00 mm2
- Top Level margin 0.10 mm2

TOTAL: 6.99mm2

7 OPERATION CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 40nm
Status pre-silicon verification
Estimated Area 7 mm^2

7.2 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			Min	Typ	Max	
Operating temperature range	T_j	-	-40	27	85	°C
Battery supply voltage	V_{BAT}	-	2.3	-	5.5	V
IO dedicated voltage	V_{IO}	-	1.62	-	3.3	V
Current consumption	I_{CC}	-	-	136.4	-	uA
		Stand-by mode	-	36.6	-	uA
Card mode receiver sensitivity		-	-	10	-	mV_{p-p}
Reader mode receiver sensitivity	V_{RED_SENS}	-	-	0.3	-	mVrms
Output transmitter power	P	-	-	2		W
DC/DC BOOST input supply voltage	V_{DCDC_BOOST}	-	2.3	-	4.8	V
DC/DC load current	I_{LOAD}	-	-	350	-	mA
DC/DC peak current	I_p	-	-	-	750	mA
DC/DC output voltage range	V_R	-	3.1	-	6	V
Quartz or external clock frequency	F_{CLK}	-	19	27.12	48	MHz

8 DELIVERABLES

File Deliverable	Format
Module layout file	GDSII format with full-layers
Reports upon GDSII generation	DRC/LVS/ERC/Antenna reports
Module circuit file	SPICE format netlist for LVS execution
Module loading/timing file	Liberty Timing File (.lib)
Module simulation model file	Verilog format
Module place and route model file	LEF format
Document (Datasheet)	PDF