Power amplifier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.13 um
- E class PA
- Frequency range 3…5 GHz
- Built-in voltage regulator
- Gain adjustment
- Portable to other technologies (upon request)

2 APPLICATIONS

- Portable transmitters
- Portable transceivers
- Mobile communication devices

3 OVERVIEW

Device is E class power amplifier (PA).
Voltage regulator is used due to transistor low breakdown voltage and PA inductive load. Such solution also provides wide range output power adjustment. Third type band-pass filter is used to provide wide bandwidth and set output impedance to 50 Ω.
The block is fabricated on iHP SiGe BiCMOS 0.13 um technology.

4 STRUCTURE

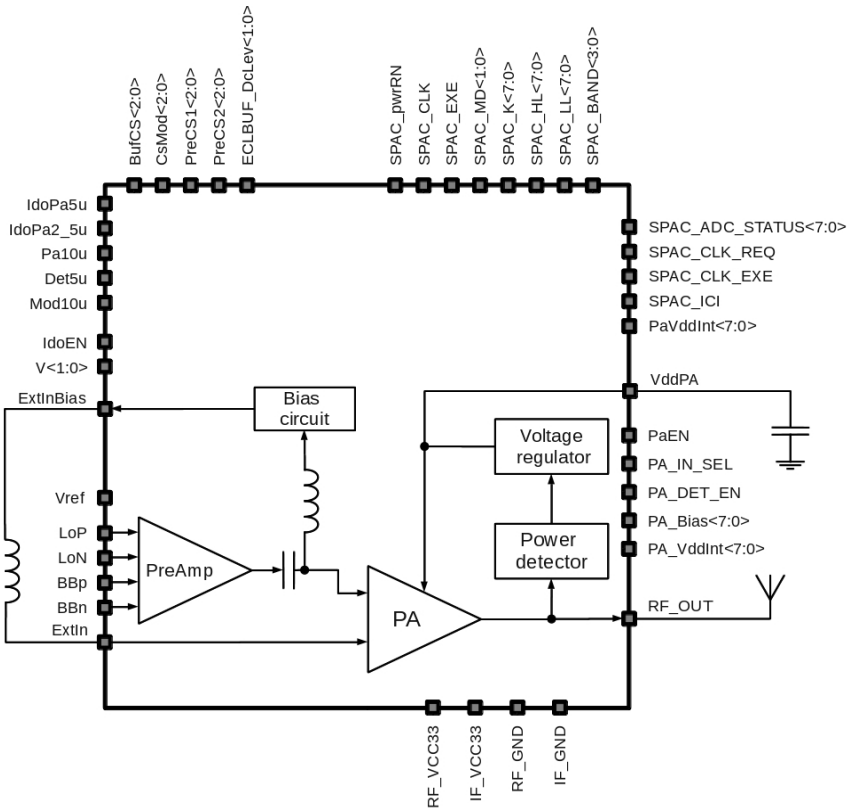

Figure 1: Power amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
IdoPa5u	IO	Voltage regulator reference current (5 uA)
IdoPa2_5u	IO	2nd voltage regulator reference current (5 uA)
Pa10u	IO	Input bias generator reference current (10 uA)
Det5u	IO	Power detector reference current
Mod10u	IO	Pre-amplifier reference current
ECLBUF_i5u	IO	Level converter reference current (5 uA)
Vref	IO	Voltage regulator reference voltage
Ext_In	I	PA External input
LoP	I	Heterodyne differential signal
LoN	I	
BBp	I	Modulating differential input
BBn	I	
extInBias	IO	External input bias
VddPa	IO	PA supply voltage external pin
RF_OUT	O	Output
BufCS<2:0>	I	Preamplifier output stage current adjustment
CsMod<2:0>	I	Preamplifier 1st stage current adjustment
Pre2CS1<2:0>	I	Preamplifier 2nd stage current adjustment
Pre2CS2<2:0>	I	Preamplifier 3rd stage current adjustment
ECLBUF_DcLev<1:0>	I	ECL buffer output bias adjustment
PaEN	I	PA enable/disable
PA_DET_EN	I	Power detector enable/disable
PA_IN_SEL	I	Input adjustment
PaBias<7:0>	I	Input bias voltage adjustment
PaVdd<7:0>	I	Output power adjustment
SPAC_pwrRN	I	Power detector power-on reset signal
SPAC_CLK	I	SPAC (System of Power AutoControl) clock frequency
SPAC_EXE	I	Cycle adjustment system of output signal
SPAC_MD<1>	I	Output power digitizing mode without voltage controller adjustment
SPAC_MD<0>	I	Finite/infinite adjustment cycle
SPAC_K<7:0>	I	Comparator levels coefficient adjustment (depends on heterodyne frequency)

Table “Pin description” (continue)

Name	Direction	Description
SPAC_HL<7:0>	I	Comparator levels upper bound
SPAC_LL<7:0>	I	Comparator levels lower bound
SPAC_BAND<3:0>	I	SPAC bandwidth
SPAC_ADC_STATUS<7:0>	O	SPAC ADC input
SPAC_CLK_REQ	O	Clock signal request
SPAC_Clear_EXE	O	SPAC stop signal
SPAC_ICI	O	SPAC shutdown indicator when achieves given number of switching
PaVddInt<7:0>	O	SPAC output voltage
IdoEN	I	Voltage regulator enable/disable
V<1:0>	I	Regulator maximum voltage adjustment
RF_VCC33	IO	RF supply voltage
IF_VCC33	IO	IF supply voltage
RF_GND	IO	RF ground
IF_GND	IO	IF ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	1200	um
Width	1240	um

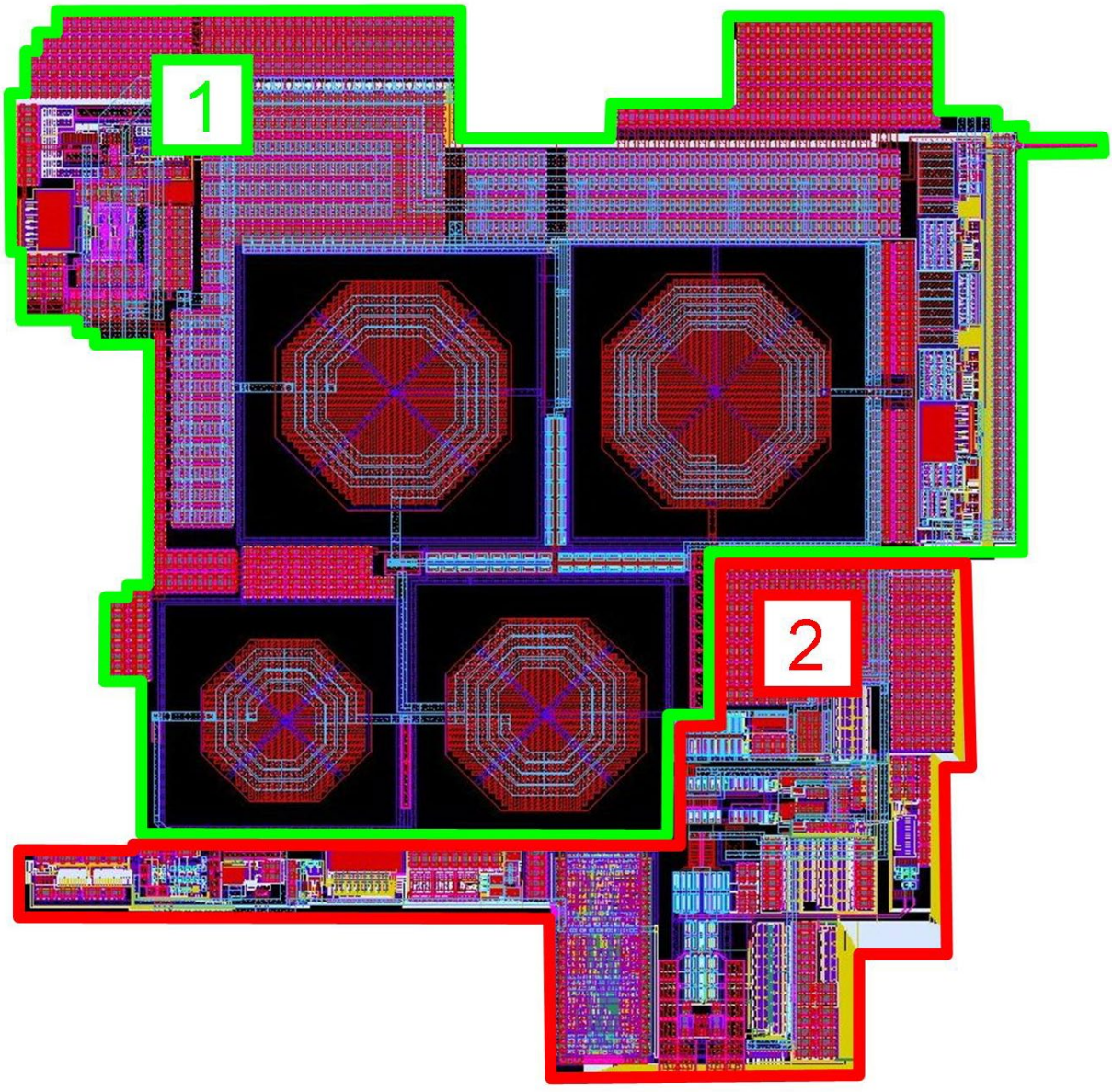

Figure 2: Device layout view

1. Power amplifier
2. Preamplifier and output signal adjustment system

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.13 um
Status _____ silicon proven
Area _____ 1.5 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.7 ÷ 3.6 V and T_a = -45 ÷ 85°C. Typical values are at V_{cc} = 3.3 V and T_a = 27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.7	3.3	3.6	V
Temperature range	T_a	-	-45	27	85	°C
Frequency range	F	-	3	-	5	GHz
PA supply voltage	V_{ddPa}	-	-	-	1.3	V
Maximum output power	P_{out_max}	F = 3 GHz	7.02	8.25	-	dBm
		F = 4 GHz	6.75	7.96	-	
		F = 5 GHz	4.99	5.31	-	
Current consumption at 5 dBm output power	I_{cons_5dBm}	F = 3 GHz	-	35.11	-	mA
		F = 4 GHz	-	33.41	-	
		F = 5 GHz	-	32.75	-	
Current consumption in a standby mode	I_{stb}	-	-	16	-	nA
2^{nd} harmonic suppression at 5 dBmW output power	ΔP_2	F = 3 GHz	-	12.6	-	dB
		F = 4 GHz	-	29.92	-	
		F = 5 GHz	-	38.37	-	
3^{rd} harmonic suppression at 5 dBmW output power	ΔP_3	F = 3 GHz	-	36.46	-	dB
		F = 4 GHz	-	58.66	-	
		F = 5 GHz	-	56.88	-	
Output impedance	R_{out}	Differential	-	50	-	Ω
Input high-level voltage	V_{IH}	Digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input low-level voltage	V_{IL}		-0.25	-	0.3	V

8 TYPICAL CHARACTERISTICS

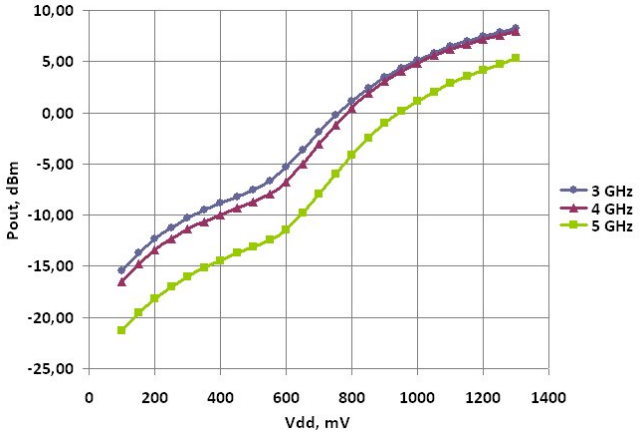

Figure 3: Output power vs supply voltage

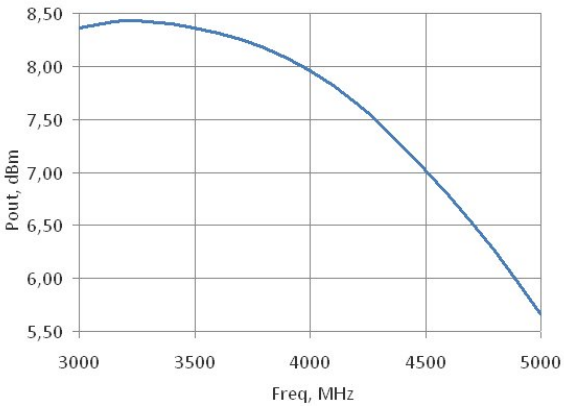

Figure 4: Output power vs frequency

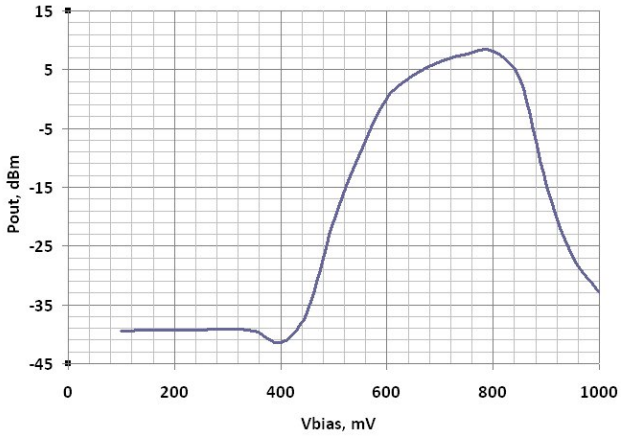

Figure 5: Output power vs bias voltage

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation