28.84 MHz Phase-frequency detector with charge pump

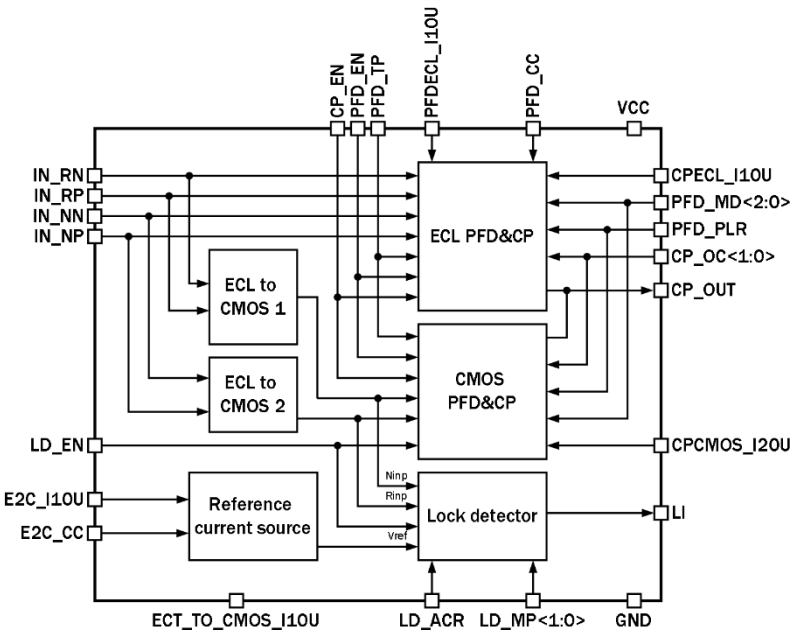
OVERVIEW

180TSMC_PFD_01 is a phase-frequency detector (PFD) forms a control signal for VCO tuning. PFD compares phases of a divided VCO signal and a divided reference oscillator signal and detects phase difference. Charge pump (CP) generates pulses for the loop filter. The structure consists of two types of PFD with CP: ECL and CMOS choosing by a bit PFD_TP. The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. LD_MP<1:0> and LD_ACR outputs set the lock monitoring period and the lock detector accuracy, respectively.

IP technology: TSMC018 SiGe BiCMOS.

IP status: silicon proven.

Area: 0.0945mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{CC}	-		3.0	3.15	3.3	V
Operating temperature range	T	-		-40	+27	+85	°C
Reference frequency	F_{REF}	-		-	24.84	-	MHz
Peak-to-peak voltage	$A_{in\ p\text{-}p}$	At the differential input		0.2	-	2.0	mV
DC operating point	V_{op}	-		V_{cc}–1.2	V_{cc}	V_{cc} -0.4	V
Output current	I_{out}	ECL PFD&CP, adjustable		20	-	97	mA
		CMOS PFD&CP, adjustable		13	-	99.5	mA
PFD reset time	t_{rst}	ECL PFD&CP		3.5	4.2	5.0	ns
		CMOS PFD&CP		1.1	1.5	2.3	ns
Lock monitoring period	MP	$T_{REF} = 1/F_{REF}$		$64\times T_{ref}$	-	$512\times T_{ref}$	us
Lock detector accuracy	ACR	ECL PFD&CP	LD_ACR = “0”	5.5	6	6.5	ns
			LD_ACR = “1”	9.6	11	12.4	
		CMOS PFD&CP	LD_ACR = “0”	5.5	6	6.5	ns
			LD_ACR = “1”	9.6	11	12.4	
Supply current	I_{cc}	ECL PFD&CP	LD_EN = “0”	1.37	1.4	1.47	mA
		CMOS PFD&CP	LD_ACR = “0”	0.17	0.18	0.2	mA
			LD_ACR = “1”	0.3	0.33	0.38	
Stand-by current	I_{stb}	ECL PFD&CP		1.7	2.2	287.7	nA
		CMOS PFD&CP		1.7	2.2	287.7	
Input logic-level high	V_{IH}	For digital inputs		$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-level low	V_{IL}			0	-	0.3	V