Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- TSMC018 SiGe BiCMOS
- Input signals with low amplitude
- Low disbalance of output current
- VCO divided signal buffering and optimization
- High accuracy
- Portable to other technologies (upon request)

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) forms a control signal for VCO tuning. PFD compares phases of a divided VCO signal and a divided reference oscillator signal and detects phase difference. Charge pump (CP) generates pulses for the loop filter.
The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. LD_MP<1:0> and LD_ACR outputs set the lock monitoring period and the lock detector accuracy, respectively.
The block is fabricated on TSMC018 SiGe BiCMOS technology.

4 STRUCTURE

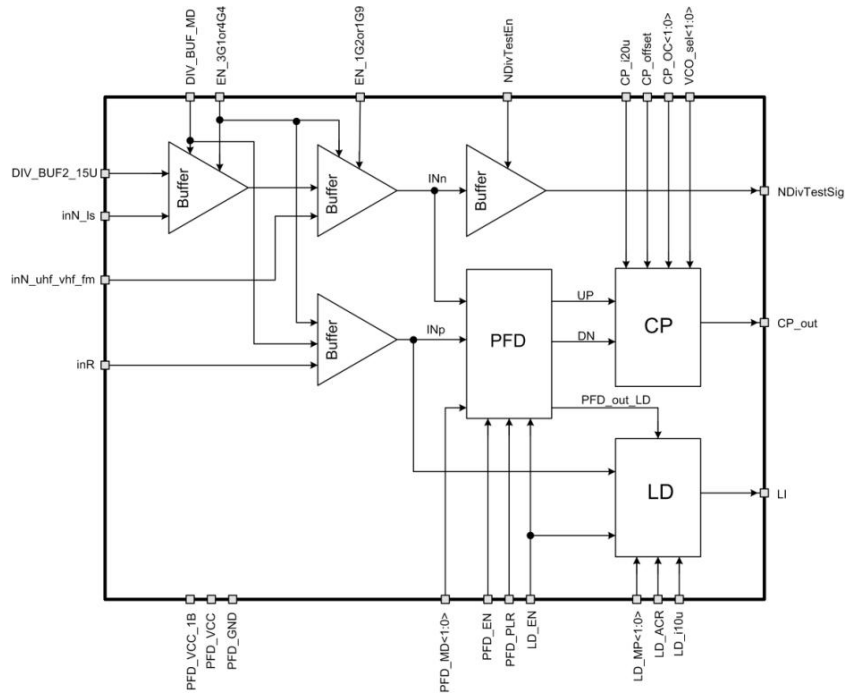

Figure 1: Phase frequency detector and charge pump structure.

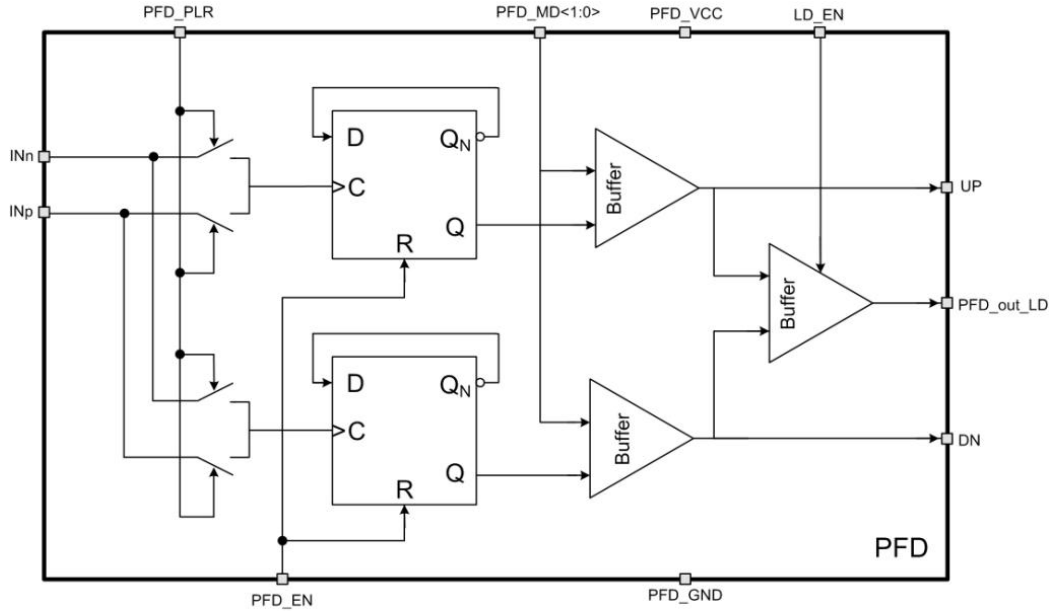

Figure 2: PFD structure.

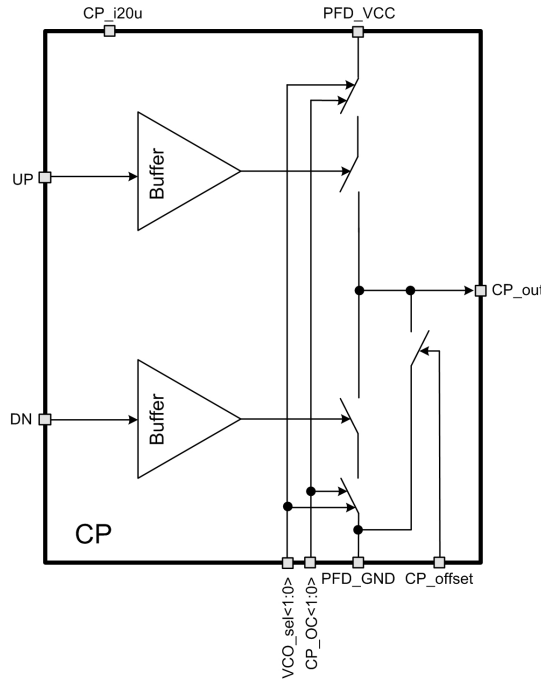

Figure 3: CP structure.

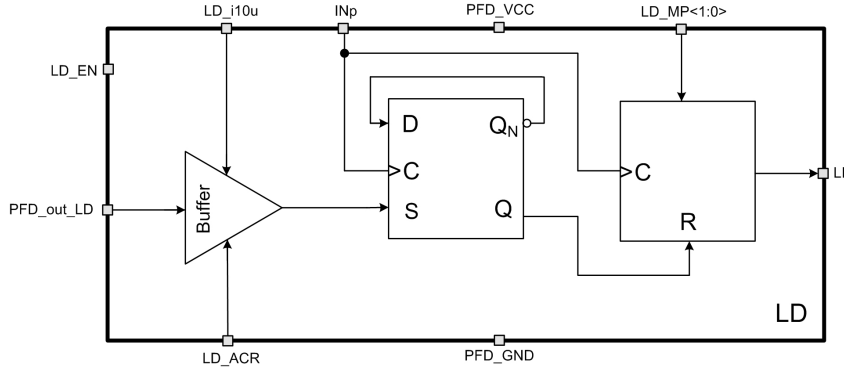

Figure 4: Lock detector structure.

5 PIN DESCRIPTION

Name	Direction	Description
CP_i20u	I	Charge pump reference current 20 µA
LD_i10u	I	Lock detector reference current 10 µA
DIV_BUF2_i5u	I	Input buffer reference current 5 µA
inN_ls	I	PLL VCO divided signal differential input
inN_uhf_vhf_fm	I	PLL VCO divided signal differential input to an input buffer
inR	I	PLL reference oscillator signal differential input
EN_1G2or1G9	I	Enable/disable of VCO divided signal mode
EN_3G1or4G4	I	Enable/disable of VCO divided signal with preliminary buffering mode
DIV_BUF_MD	I	Enable/disable of VCO divided signal optimization mode
PFD_EN	I	PFD enable/disable
LD_EN	I	Lock detector enable/disable
PFD_PLR	I	PFD polarity
PFD_MD<2:0>	I	Phase detector reset circuit control
CP_OC<1:0>	I	Charge pump output current control
VCO_sel<1:0>		
CP_offset	I	Adjustment mode of control voltage discharging current: 0 normal 1 current increasing by 20 µA
LD_MP<1:0>	I	Lock monitoring period control
LD_ACR	I	Lock detector accuracy control
V_{ctrl}	O	Charge pump output
LI	O	Lock indicator output
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

Dimension	Value	Unit
Height	300	µm
Width	1050	µm

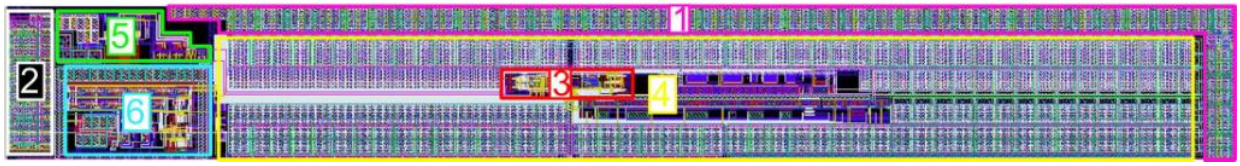

Figure 1: PFD and CP layout view.

1. Ground bus and supply voltage bus with filter capacitors
2. Supply voltage bus with filter capacitors (1.8 V)
3. Phase-frequency detector
4. Charge pump
5. VCO divided signal input buffer
6. Lock detector

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe
Status _____ Silicon proven
Area _____ 0.095 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.8 ÷ 3.6 V и T = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.7 V, T = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{CC}	-	2.8	2.7	3.6	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	F_{ref}	-	0.32	2.0	10	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p\text{-}p}$	For inputs inN_ls, inN_uhf_vhf_fm, inR	0	-	4.5	mV
Output current	I_{out}	Preset 1	46.0	46.5	48.0	mA
		Preset 2	51.0	51.5	53.5	
		Preset 3	66.5	67.0	69.5	
		Preset 4	76.5	77.5	80.0	
		Preset 5	91.5	92.5	95.5	
		Preset 6	102.0	103.0	106.0	
		Preset 7	132.0	133.5	138.0	
		Preset 8	152.5	154.0	159.0	
		Preset 9	182.0	184.0	190.0	
		Preset 10	202.0	204.0	210.5	
		Preset 11	261.5	263.5	272.5	
		Preset 12	300.5	303.0	313.0	
		Preset 13	362.5	366.0	376.5	
		Preset 14	402.5	406.0	417.5	
		Preset 15	521.0	525.0	540.0	
		Preset 16	599.0	603.5	635.0	
PFD reset time	t_{rst}	-	1.8	2.8	3.3	ns
Lock monitoring period	MP	$T_{ref} = \frac{1}{F_{ref}}$	64×T_{ref}	-	512×T_{ref}	µs
Lock detector accuracy	ACR	Preset 21	5.5	6	6.5	ns
		Preset 22	9.5	10.5	12	
Supply current	I_{cc}	Preset 17	306.0	317.5	348.0	mA
		Preset 18	345.5	363.0	402.5	
		Preset 19	323.0	335.5	371.5	
		Preset 20	307.5	319.5	350.5	
Stand-by current	I_{stb}	-	27	1.0	27.0	nA
Input logic-level high	V_{IH}	For digital inputs	0.7V_{cc}	-	V_{cc} + 0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

Table 2: Presets description.

Presets name	Control signal values		Notes
Preset 1	VCO_sel = “00”	CP_OC = “00”	CP output current control
Preset 2	VCO_sel = “01”	CP_OC = “00”	
Preset 3	VCO_sel = “10”	CP_OC = “00”	
Preset 4	VCO_sel = “11”	CP_OC = “00”	
Preset 5	VCO_sel = “00”	CP_OC = “01”	
Preset 6	VCO_sel = “01”	CP_OC = “01”	
Preset 7	VCO_sel = “10”	CP_OC = “01”	
Preset 8	VCO_sel = “11”	CP_OC = “01”	
Preset 9	VCO_sel = “00”	CP_OC = “10”	
Preset 10	VCO_sel = “01”	CP_OC = “10”	
Preset 11	VCO_sel = “10”	CP_OC = “10”	
Preset 12	VCO_sel = “11”	CP_OC = “10”	
Preset 13	VCO_sel = “00”	CP_OC = “11”	
Preset 14	VCO_sel = “01”	CP_OC = “11”	
Preset 15	VCO_sel = “10”	CP_OC = “11”	
Preset 16	VCO_sel = “11”	CP_OC = “11”	
Preset 17	EN_1G2or1G9 = “0”	LD_EN = “0”	VCO divided signal mode. LD is disabled.
	EN_3G1or4G4 = “1”	DIV_BUF_MD = “0”	
Preset 18	EN_1G2or1G9 = “0”	LD_EN = “1”	VCO divided signal mode. LD is enabled.
	EN_3G1or4G4 = “1”	DIV_BUF_MD = “0”	
Preset 19	EN_1G2or1G9 = “0”	LD_EN = “0”	VCO divided signal buffering mode. LD is disabled.
	EN_3G1or4G4 = “1”	DIV_BUF_MD = “0”	
Preset 20	EN_1G2or1G9 = “0”	LD_EN = “0”	VCO divided signal optimization mode. LD is disabled.
	EN_3G1or4G4 = “1”	DIV_BUF_MD = “1”	
Preset 21	LD_ACR = “0”		Lock detector accuracy control
Preset 22	LD_ACR = “1”		

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation