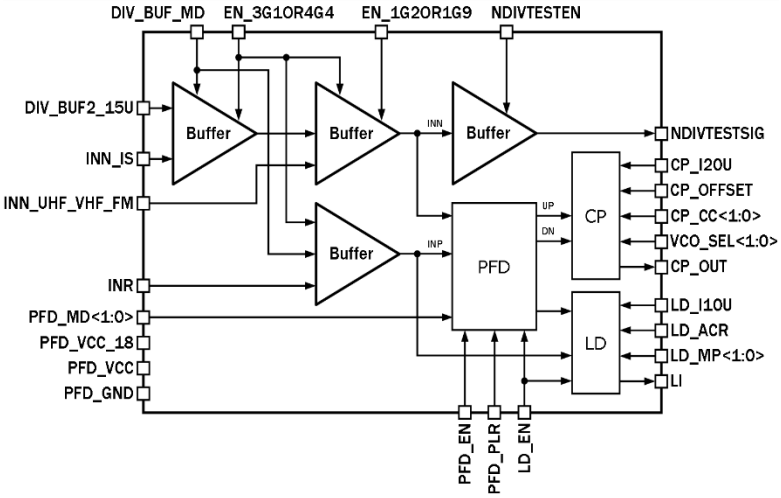
0.32 to 10 MHz Phase-frequency detector

OVERVIEW

180TSMC_PFD_02 is a phase-frequency detector (PFD) forms a control signal for VCO tuning. PFD compares phases of a divided VCO signal and a divided reference oscillator signal and detects phase difference. Charge pump (CP) generates pulses for the loop filter. The lock detector monitors the current status of PLL by comparing the phase difference of VCO divided signal and reference oscillator signal with required value. LD_MP<1:0> and LD_ACR outputs set the lock monitoring period and the lock detector accuracy, respectively.
IP technology: TSMC018 SiGe BiCMOS.
IP status: silicon proven.
Area: 0.315mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{CC}	-		2.8	2.7	3.6	V
Operating temperature range	T_j	-		-40	+27	+85	°C
Reference frequency	F_{REF}	-		0.32	2.0	10	MHz
Peak-to-peak voltage	$A_{in\ p\text{-}p}$	At the differential input		0	-	4.5	mV
Output current	I_{out}	CP_OC = "00"	VCO_sel = "00"	46.0	46.5	48.0	mA
			VCO_sel = "01"	51.0	51.5	53.5	
			VCO_sel = "10"	66.5	67.0	69.5	
			VCO_sel = "11"	76.5	77.5	80.0	
		CP_OC = "01"	VCO_sel = "00"	91.5	92.5	95.5	
			VCO_sel = "01"	102.0	103.0	106.0	
			VCO_sel = "10"	132.0	133.5	138.0	
			VCO_sel = "11"	152.5	154.0	159.0	
		CP_OC = "10"	VCO_sel = "00"	182.0	184.0	190.0	
			VCO_sel = "01"	202.0	204.0	210.5	
			VCO_sel = "10"	261.5	263.5	272.5	
			VCO_sel = "11"	300.5	303.0	313.0	
		CP_OC = "11"	VCO_sel = "00"	362.5	366.0	376.5	
			VCO_sel = "01"	402.5	406.0	417.5	
			VCO_sel = "10"	521.0	525.0	540.0	
			VCO_sel = "11"	599.0	603.5	635.0	
PFD reset time	t_{rst}	-		1.8	2.8	3.3	ns
Lock monitoring period	MP	$T_{REF} = 1/F_{REF}$		$64\times T_{ref}$	-	$512\times T_{ref}$	us
Lock detector accuracy	ACR	LD_ACR = "0"		5.5	6	6.5	ns
		LD_ACR = "1"		9.5	10.5	12	
Supply current	I_{cc}	VCO divided signal mode, LD is disabled		306.0	317.5	348.0	mA
		VCO divided signal mode, LD is enabled		345.5	363.0	402.5	
		VCO divided signal buffering mode, LD is disabled		323.0	335.5	371.5	
Stand-by current	I_{stb}	-		27	1.0	27.0	nA
Input logic-level high	V_{IH}	For digital inputs		$0.7V_{cc}$	-	$V_{cc}+0.25$	V
Input logic-level low	V_{IL}			-0.25	-	0.3	V