Phase frequency detector and charge pump

SPECIFICATION

1 FEATURES

- TSMC018 SiGe 0.18µm
- Input signals with low amplitude
- Low disbalance of output current
- Portable to other technologies (upon request)

2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Phase-frequency detector (PFD) forms control signal for VCO tuning. PFD compares phases of divided VCO signal and divided reference oscillator signal and detects phase difference. Charge pump generates pulses for loop filter.
The block is fabricated on TSMC018 SiGe 0.18µm technology.

4 STRUCTURE

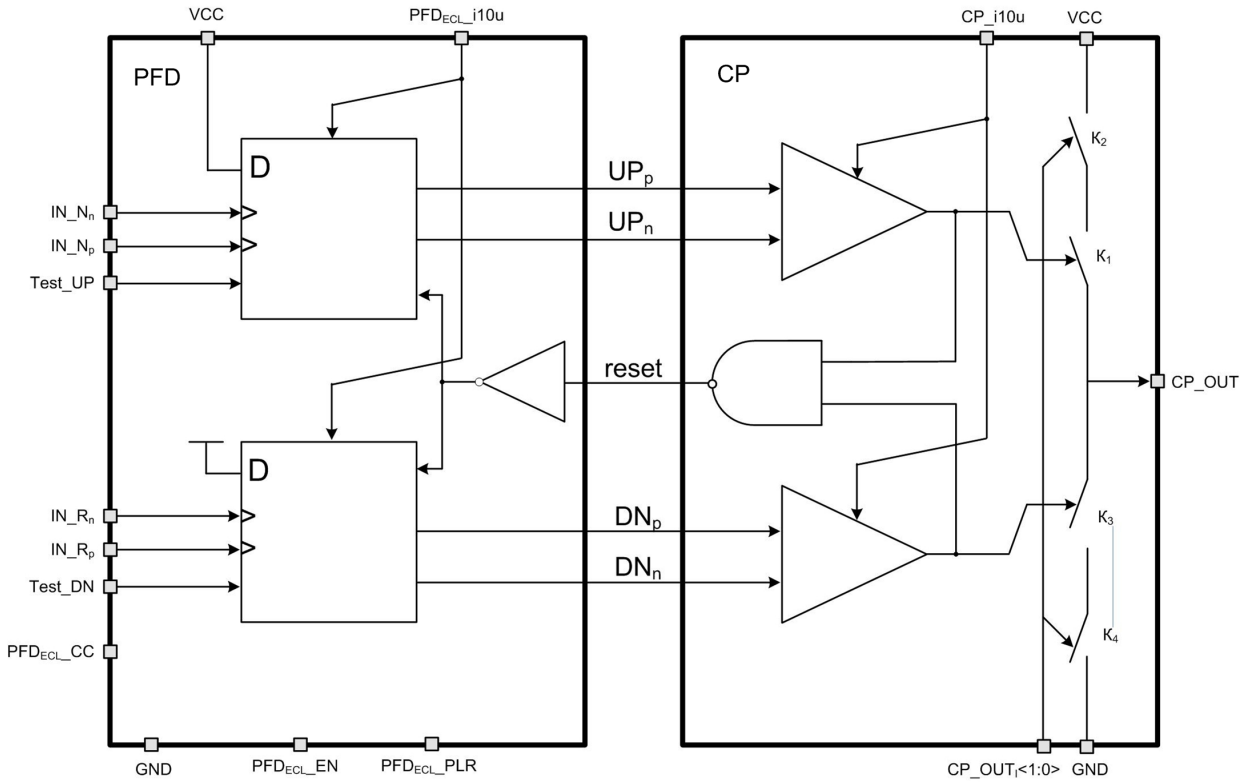

Figure 1: Phase frequency detector and charge pump structure

5 PIN DESCRIPTION

Name	Direction	Description
PFD_{ECL}_i10u	IO	PFD reference current
CP_i10u	IO	CP reference current
IN_N_p	I	PLL VCO divided signal differential input
IN_N_n		
IN_R_p	I	PLL reference oscillator signal differential input
IN_R_n		
PFD_{ECL}_EN	I	PFD and CP enable/disable
PFD_{ECL}_PLR	I	PFD polarity
PFD_{ECL}_CC	I	PFD current consumption control
Test_UP	I	Enable/disable of PFD up static current test mode
Test_DN	I	Enable/disable of PFD down static current test mode
CP_OUT	IO	CP output
CP_OUT_I<1:0>	I	Output current adjustment
GND	IO	Ground
VCC	IO	Supply voltage

6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

Table 1: Blocks dimensions.

Dimension	Value	Unit
Height	248	µm
Width	205	µm

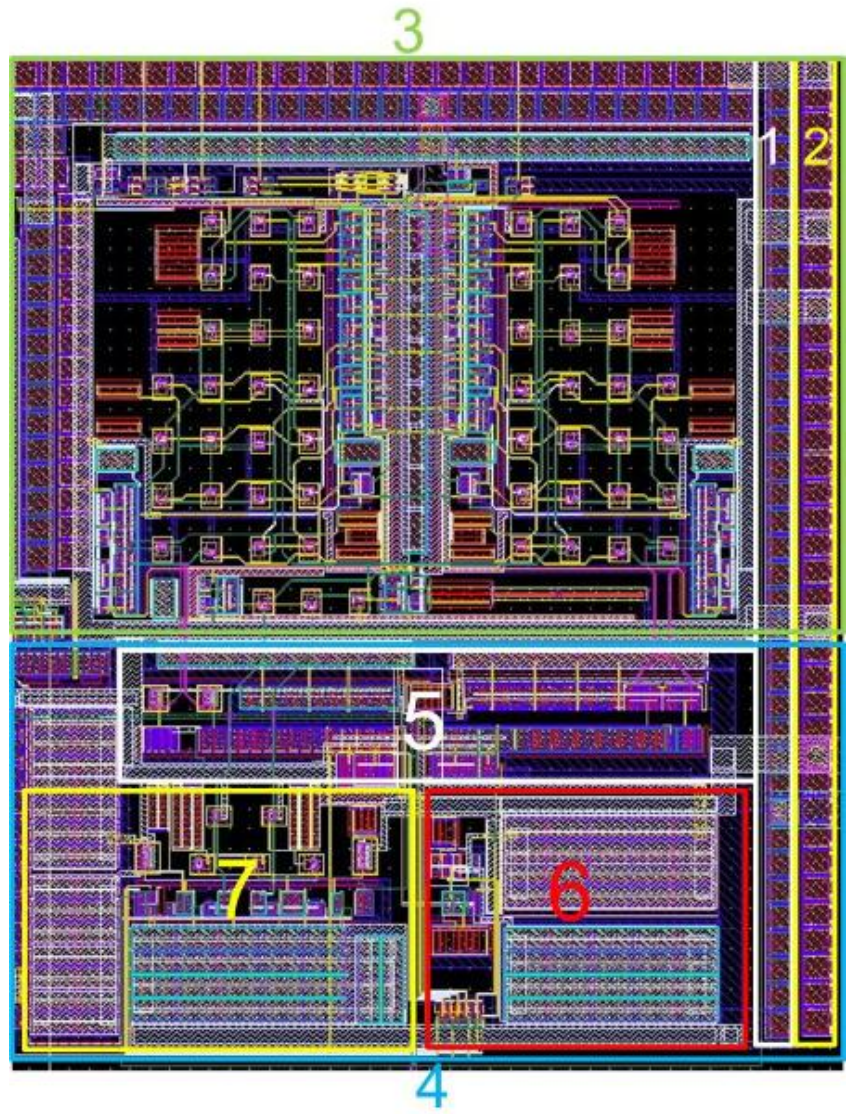

Figure 2: PFD and CP layout view

1. Ground bus with filter capacitors
2. Supply voltage bus with filter capacitors
3. Phase detector
4. Charge pump
5. Charge pump output stage
6. Reference voltage source
7. PFD reset circuit

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC018 SiGe
Status _____ silicon proven
Area _____ 0.05 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 3.0 ÷ 3.3 V и T = -40 ÷ +85 °C. Typical values are at V_{cc} = 3.15 V, T = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{CC}	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	F_{ref}	-	-	24.84	-	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p\text{-}p}$	For inputs IN_p, IN_n, IN_R_p и IN_R_n	0.2	-	2.0	V
DC operating point	V_{op}		V_{cc} – 1.2	-	V_{cc} – 0.2	V
Output current	I_{out}	Preset 1	20.5	21.0	21.5	µA
		Preset 2	40.5	41.0	42.5	
		Preset 3	81.0	82.0	85.0	
		Preset 4	101.0	102.5	106.0	
PFD reset time	t_{rst}	-	4.4	4.85	5.75	ns
PFD input amplitude	A_{in}	-	150	200	210	mV
Supply current	I_{cc}	-	1.37	1.44	1.61	mA
Stand-by current	I_{stb}	-	0.2	1.5	3.6	nA
Input logic-level high	V_{IH}	For digital inputs PFD_{ECL}_EN, CP_OUT_I<1:0>	0.7V_{cc}	-	V_{cc} + 0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation