Charge pump

SPECIFICATION

1 FEATURES

- AMS035 BiCMOS 0.35 um technology
- Adjustable output current
- Phase-frequency detector (PFD) reset circuit
- Differential input signal
- Input signal frequency up to 100 MHz
- Portable to other technologies (upon request)

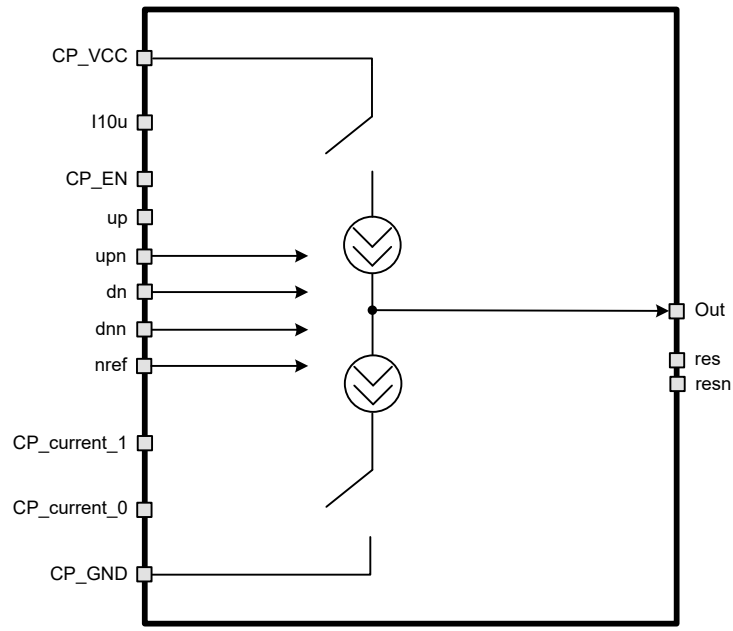
2 APPLICATION

- Phase-locked loop synthesizer

3 OVERVIEW

Charge pump (CP) is a switched current sources controlled by phase-frequency detector which inject or remove some charge to increase or decrease VCO control voltage depended on phase difference between reference frequency and divided VCO frequency.
The block is fabricated on AMS035 BiCMOS 0.35 um technology.

4 STRUCTURE



5 PIN DESCRIPTION

Name	Direction	Description
I10u	I	Reference current (10 mkA)
CP_EN	I	Enable/disable charge pump
up	I	Analog differential increase output voltage signal
upn	I	
dn	I	Analog differential decrease output voltage signal
dnn	I	
res	O	PFD reset signal output
resn	O	
CP_current_0	I	Output current preset
CP_current_1	I	Output current preset
nref	I	Current supply reference voltage n-MOS
out	O	Charge pump output
CP_VCC	IO	Supply voltage
CP_GND	IO	Ground

6 LAYOUT DESCRIPTION

The block charge pump dimensions are given in the table 6.1.

Table 6.1: Block dimensions.

Dimension	Value	Unit
Height	130	um
Width	480	um

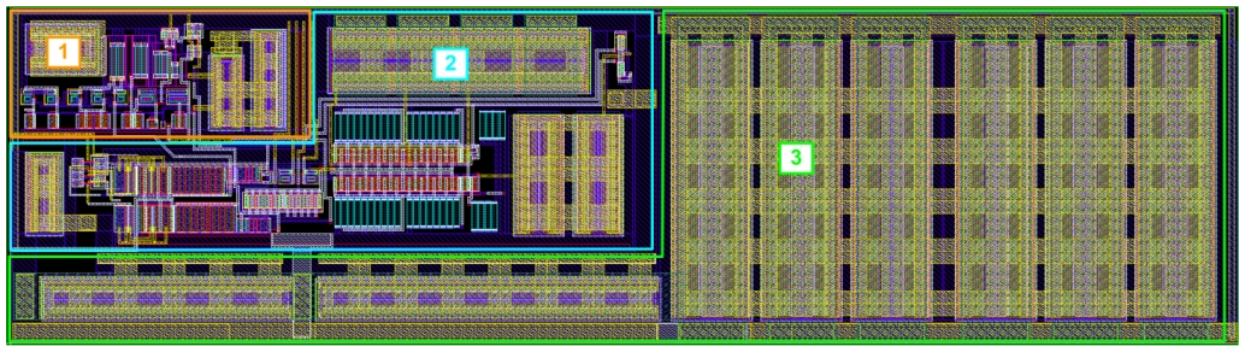


Figure 6.1: Charge pump layout view

1 PFD reset circuit
2 Current sources
3 Filter capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS 0.35 um
Status silicon proven
Area 0.063 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = +2.6 ÷ +3.15 V, T = -40 ÷ +85 °C. Typical values are at V_{cc} = +2.7 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.65	2.7	3.15	V
Operating temperature range	T	-	-40	27	85	°C
Input signal frequency	F_{max}	-	-	-	100	MHz
Source current	$I_{out\ up}$	V_{out}= 0.4..V_{cc}-0.4	19.2	20.4	21.1	µA
			36.6	38.7	40	
			71.2	75.3	77.8	
			88.6	93.6	96.7	
Sink current	$I_{out\ dn}$	V_{out}= 0.4..V_{cc}-0.4	19.4	20	20.4	µA
			38	39.1	39.9	
			75.3	77.3	78.8	
			93.9	96.5	98.3	
Working output voltage range	V_{out}	-	0.4	-	V_{cc}-0.4	V
Supply current	I_{dd}	-	-	0.5	-	mA
Stand-by current	I_{st}	-	-	-	20	nA
Input logic-level high	V_{OH}	-	0.9V_{cc}	-	V_{cc}	V
Input logic-level low	V_{OL}	-	-0.2	0	0.2	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section “Technical characteristics” (refer to page 4)