

# Phase frequency detector and charge pump

## SPECIFICATION

### 1 FEATURES

- AMS035 BiCMOS 0.35  $\mu\text{m}$
- Input signals with low amplitude
- Low disbalance of output current
- Portable to other technologies (upon request)

### 2 APPLICATION

- Phase-locked loop synthesizer

### 3 OVERVIEW

Phase-frequency detector (PFD) forms a control signal for VCO tuning. PFD compares phases of a divided VCO signal and a divided reference oscillator signal and detects phase difference. Charge pump generates pulses for the loop filter.

The block is fabricated on AMS035 BiCMOS 0.35  $\mu\text{m}$  technology.

### 4 STRUCTURE

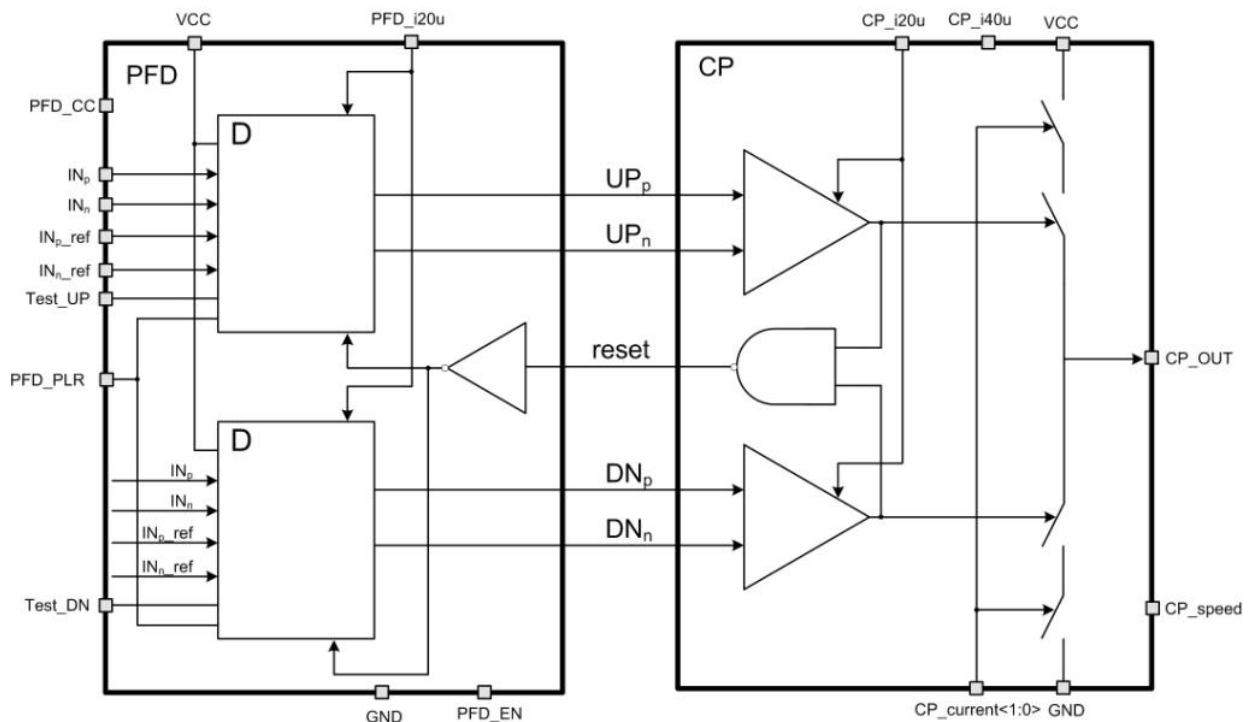


Figure 1: Phase frequency detector and charge pump structure

## 5 PIN DESCRIPTION

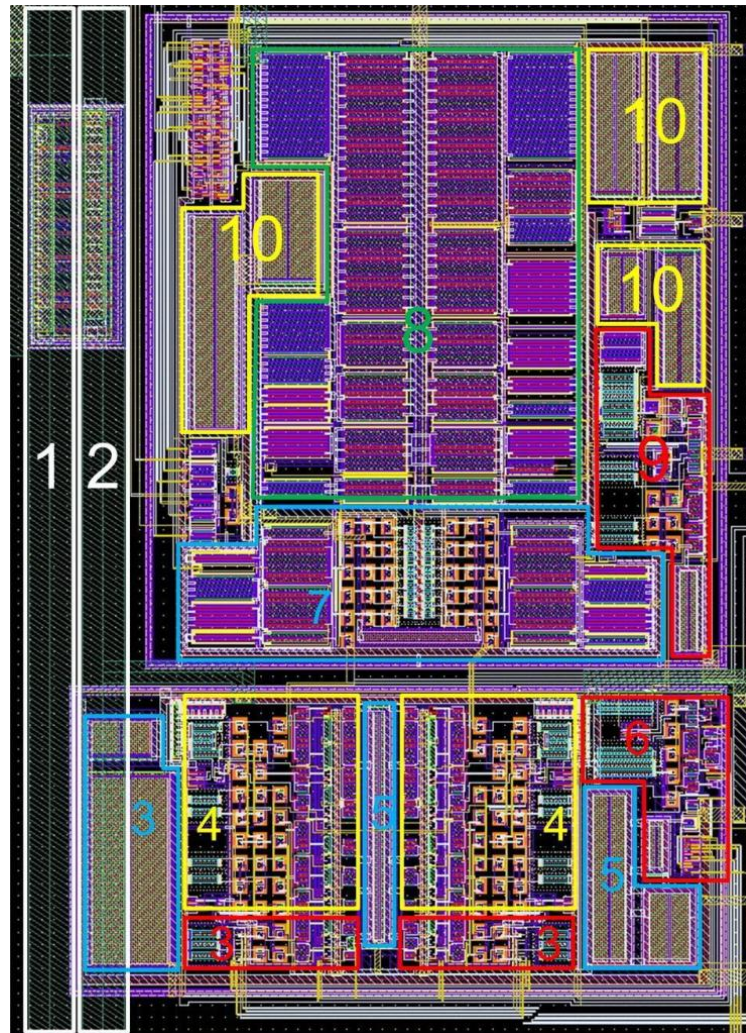
Name	Direction	Description
PFD_i20u	IO	PFD reference current 20 $\mu$ A
CP_i20u	IO	Charge pump reference current 20 $\mu$ A
CP_i40u	IO	Charge pump reference current 40 $\mu$ A
IN <sub>p</sub>	I	PLL VCO divided signal differential input
IN <sub>n</sub>		
IN <sub>p_ref</sub>	I	PLL reference oscillator signal differential input
IN <sub>n_ref</sub>		
PFD_EN	I	PFD and charge pump enable/disable
PFD_PLR	I	PFD polarity
PFD_CC	I	PFD current consumption control
Test_UP	I	Enable/disable of PFD up static current test mode
Test_DN	I	Enable/disable of PFD down static current test mode
CP_current<1:0>	I	Charge pump output current control
CP_speed	I	Charge pump response speed control
CP_OUT	O	Charge pump output
GND	IO	Ground
VCC	IO	Supply voltage

## 6 LAYOUT DESCRIPTION

Frequency-phase detector and charge pump dimensions are given in the table 1.

**Table 1:** Blocks dimensions.

Dimension	Value	Unit
Height	470	$\mu\text{m}$
Width	300	$\mu\text{m}$



**Figure 2:** PFD and CP layout view

- 1 PFD ground bus
- 2 PFD supply voltage bus
- 3 PFD input buffer
- 4 PFD triggers
- 5 PFD filter capacitors
- 6 PFD reset circuit
- 7 Charge pump input buffer
- 8 Charge pump output stage
- 9 Signal former for phase detector reset circuit
- 10 Charge pump filter capacitors

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ AMS035 BiCMOS 0.35  
 Status \_\_\_\_\_ Silicon proven  
 Area \_\_\_\_\_ 0.15 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.85 \div 3.15$  V and  $T = -40 \div +85$  °C. Typical values are at  $V_{cc} = 3.0$  V,  $T = +27$  °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{CC}$	-	3.0	3.15	3.3	V
Operating temperature range	T	-	-40	+27	+85	°C
Reference frequency	$F_{ref}$	-	-	1	20	MHz
Peak-to-peak voltage at the differential input	$A_{in\ p-p}$	For inputs $IN_p$ , $IN_n$ , $IN_{p\_ref}$ and $IN_{n\_ref}$	400	-	700	mV
DC operating point	$V_{op}$		$V_{cc} - 1.0$	-	$V_{cc} - 0.3$	V
Output current	$I_{out}$	Preset 1	0.59	0.66	0.69	mA
		Preset 2	2.34	2.64	2.73	
		Preset 3	1.17	1.32	1.37	
		Preset 4	2.92	2.2	2.42	
		Preset 5	0.9	1.27	1.34	
		Preset 6	3.6	5.04	5.32	
		Preset 7	1.8	4.02	2.67	
		Preset 8	4.5	6.3	6.66	
PFD reset time	$t_{rst}$	-	2.05	4.58	6.73	ns
Supply current	$I_{cc}$	-	2.88	3.23	4.44	mA
Stand-by current	$I_{stb}$	-	0.45	0.6	150	nA
Input logic-level high	$V_{IH}$	For digital inputs	$0.7V_{cc}$	-	$V_{cc} + 0.25$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation