25MHz to 4.0GHz Fractional-N RC PLL Synthesizer

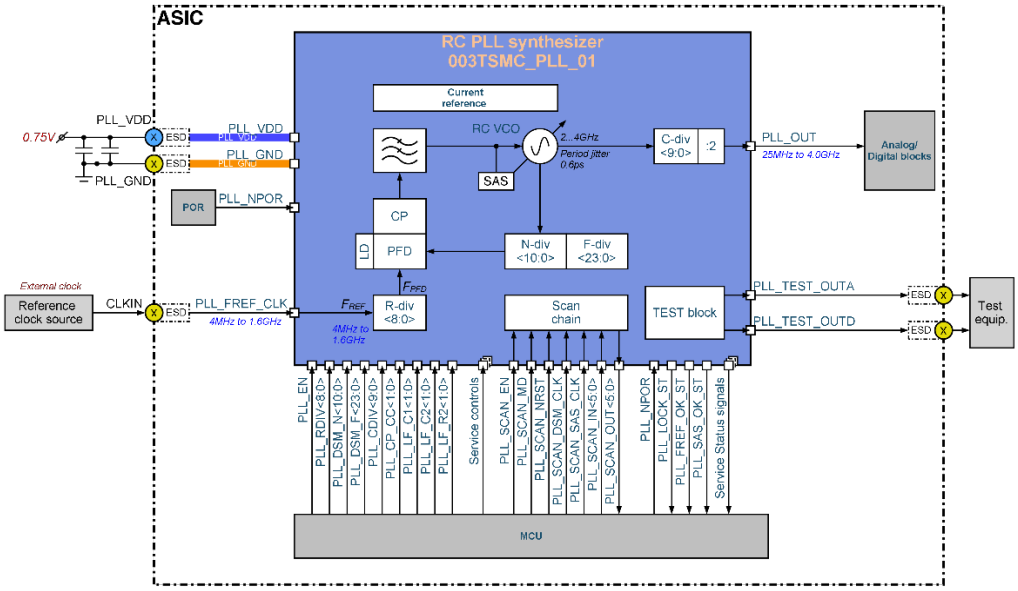
OVERVIEW

Fractional-N Phase locked loop frequency synthesizer is intended for ASIC clock generation.

The Fractional-N PLL loop with 2GHz-4GHz VCO has high phase noise performance and ultra-fine frequency tuning step.

VCO Sub-band auto select (SAS) system allows to find automatically appropriate sub-band for VCO on locked PLL.

The block embeds reference current sources.



IP technology: TSMC 3nm N3P.
IP status: pre-silicon verified.
Silicon area: 0.01254mm^2 (108um x 115um)

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Units
				min	t	max	
Supply voltage	PLL_VDD	-		0.675	0.75	0.825	V
Operating temperature range	T_j	Junction		-40	27	125	ºC
Output frequency	F_{out}	-		25	-	4000	MHz
Phase noise	LO_{PN}	F_{out}= 4GHz	at 10MHz	-	-107	-	dBc/Hz
			at 100MHz		-127	-	
			at 1GHz	-	-147	-	
Output clock period jitter	J_{period}	-		-	0.6	-	ps
Reference frequency	F_{ref}	-		4.0	-	1600	MHz
Lock time	T_{lock}	-		-	50	-	us
Start-up time	T_{start}	-		-	3.1	-	ms
Output frequency fine tuning range	A	From center frequency		-1000	-	1000	ppm
LO duty cycle	LO_{DC}	-		45	-	55	%
Current consumption	I_{cc}	F_{out}= 4GHz		-	3.0	5.0	mA
Shutdown current	I_{std}	-		-	15	900	uA
Reference signal - high level	V_{RefH}	CMOS		PLL_VDD-0.1	-	PLL_VDD	V
Reference signal - low level	V_{RefL}			0	-	0.1	