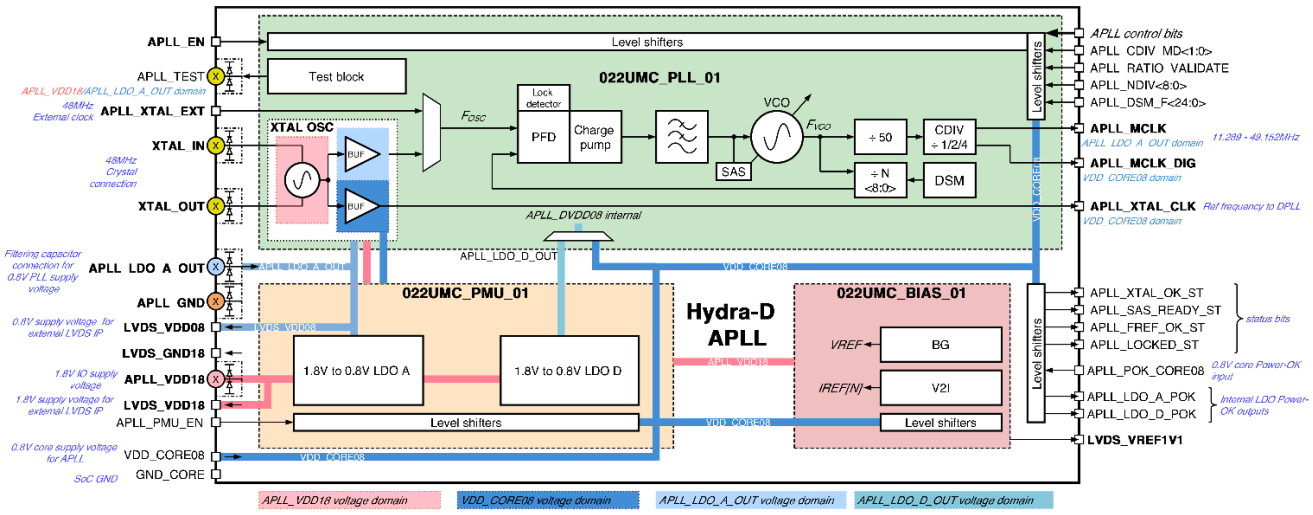
10MHz to 50MHz Fractional-N PLL Synthesizer

OVERVIEW

APLL Fractional-N phase locked loop frequency synthesizer is intended for SoC clock generation and embeds a reference 10MHz – 50MHz XTAL oscillator, which is also able to work as an input signal buffer in the same frequency range. The internal 2.5GHz high frequency VCO provides both excellent phase noise performance and ultra-fine frequency tuning step. The PLL is supplied from 1.8V input voltage down converted by embedded LDOs with low noise and high PSRR. The embedded Bias block provides a low noise and high PSRR voltage and current references to PMU, PLL core and XTAL blocks, as well as it outputs a voltage reference 1.0V for external purposes with up to 10uA load.



IP technology: UMC 22nm ULP.
IP status: silicon proven.
Silicon area: 0.95mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{DD18}	-	1.71	1.8	1.89	V
	V_{DD_CORE08}	-	0.72/0.9	0.8/1.0	0.88/1.05	V
Operating temperature range	T_j	Junction	-40	27	125	ºC
Output frequency	F_{out}	Mode1	-	11.2896	-	MHz
		Mode 2	-	12.2880	-	
		Mode 3	-	22.5792	-	
		Mode 4	-	24.5760	-	
		Mode 5	-	45.1584	-	
		Mode 6	-	49.1520	-	
Phase noise	LO_{PN}	at 1 MHz	-	-117	-	dBc/Hz
Output clock RMS jitter	J_{RMS}	10Hz–10MHz	-	-	2	ps
Reference frequency	F_{ref}	-	10	48	50	MHz
Lock time	T_{lock}	-	-	-	10	us
Output frequency fine tuning range	A	Fine tuning step 1ppb	-1000	-	1000	ppm
LO duty cycle	LO_{DC}	-	48	-	51	%
Current consumption	I_{cc}	F_{out} = 400 MHz	160	210	250	uA
		F_{out} = 800 MHz	350	410	450	
Current consumption in standby mode	I_{stb}	-	-	0.03	2.7	uA
Reference signal - high level	V_{RefH}	CMOS	V_{DD_CORE08} -0.1	-	V_{DD_CORE08}	V
Reference signal - low level	V_{RefL}		0	-	0.1	