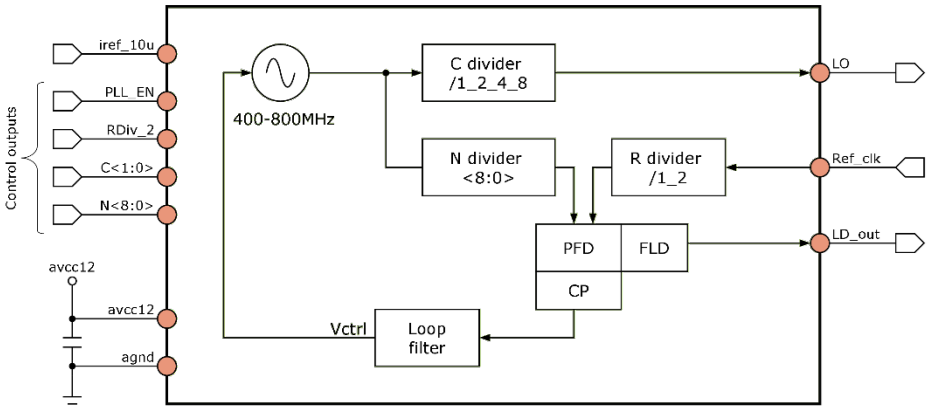
50-800MHz phase-locked loop frequency synthesizer

OVERVIEW

055TSMC_PLL_01 is an integer-N phase-locked loop frequency synthesizer (PLL), which produces stable clock signal in range from 50 to 800MHz. It works with reference frequency from 4 to 20 MHz. The block includes 400-800MHz VCO, programmable N and R dividers, low noise digital phase-frequency detector (PFD), charge pump (CP) with integrated loop filter, frequency lock detector (FLD) and programmable output clock C divider.



IP technology: TSMC CMOS 55nm.

IP status: silicon proven.

Silicon area: 0.007 mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions			Value min	Value typ.	Value max	Units
Supply voltage	V_{avcc12}	-			1.08	1.2	1.32	V
Operating temperature range	T_j	-			-45	25	+85	°C
Reference current	I_{ref}	-			-	10	-	µA
Current consumption	I_{cc}	F_{LO} = 40MHz			-	200	300	µA
		F_{LO} = 800MHz			-	280	370	
Current consumption in standby mode	I_{stb}	-			-	0.03	2.4	µA
Input logic-level high	V_{IH}	For digital inputs			Vavcc12-0.25	-	Vavcc12	V
Input logic-level low	V_{IL}				0	-	0.25	V
Reference frequency range	F_{ref_clk}	-			4	-	20	MHz
Output frequency	F_{LO}	-			50	200	800	MHz
Phase noise	LO_{PN}	F_{ref} = 10MHz; F_{LO} = 200MHz		@1MHz	-	-93.5	-	dBc/Hz
		F_{ref_clk} = 6MHz	F_{LO} = 200MHz	@10kHz	-	-103.6	-	
				@100kHz	-	-101.7	-	
				@1MHz	-	-102.2	-	
			F_{LO} = 200MHz	@10kHz	-	-98.2	-	
				@100kHz	-	-95.7	-	
				@1MHz	-	-92.9	-	
LO duty cycle	LO_{DC}	-			40	50	60	%
Ref_clk duty cycle	Ref_clk_{DC}	-			40	50	60	%
LO RMS jitter value	J_{RMS}	F_{ref} = 10MHz; F_{LO} = 200MHz; Ref_clk RMS jitter < 5ps; no other noisy devices on the synthesizer power supply			-	35	-	ps
		F_{ref} = 6MHz	F_{LO} = 200MHz		-	28	-	
			F_{LO} = 400MHz		-	21	-	
N dividing ratio	N	-			16	-	511	-
C dividing ratio	C	-			1	-	8	-
R dividing ratio	R	-			1	-	2	-
Lock time	T_{lock}	-			-	40	-	µs
Lock detector accuracy	S_{err}	-			-	5	-	ns