Wide band 3.5 GHz -7 GHz low noise PLL synthesizer

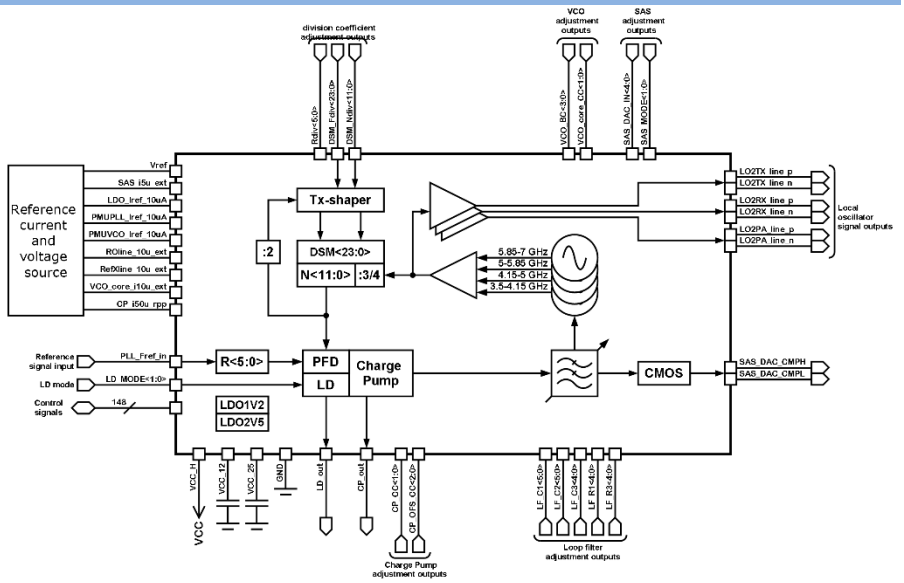
OVERVIEW

055TSMC_PLL_02 is a PLL frequency synthesizer that generates a high-frequency signal in the range from 3.5 GHz to 7 GHz. The synthesizer consists of 4 voltage-controlled oscillators (VCO) with internal LC circuit and automatic subband selection system; a digital phase-frequency detector (PFD); a precision charge pump (CP) with integrated adjustable loop filter; a programmable divider of reference signal and a system of programmable feedback dividers controlled by a delta-sigma modulator (DSM).

IP technology: TSMC CMOS 55nm.

IP status: silicon proven.

Silicon area: 2.4 mm^2



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Unit
Supply voltage	V_{CC_H}	-		2.25	2.5	3.3	V
	V_{CC_25}	-		2.25	2.5	2.75	
	V_{CC_12}	-		1.08	1.2	1.32	
Temperature range	T_j	-		-40	+25	+85	°C
Current consumption	I_{CC}	Active mode, V_{CC_H} = 2.5 V		-	30	-	mA
Input reference frequency	F_{ref}	-		5	-	50	MHz
Output frequency	F	-		3.5	-	7	GHz
Output frequency tuning step	ΔF	Comparison frequency is 50 MHz		3	-	-	Hz
VCO frequency range	F_{VCO}	7 GHz core		5.85	-	7.00	GHz
		5.8 GHz core		5.00	-	5.85	
		5 GHz core		4.15	-	5.00	
		4.1 GHz core		3.50	-	4.15	
Phase noise	PN	F = 6 GHz, F_{ref} = 50 MHz	@10 kHz	-	-97	-	dBc/Hz
			@100 kHz	-	-97	-	
			@1 MHz	-	-117	-	
Jitter value	J_{RMS}	F = 6 GHz		-	350	-	fs
Input logic-high level	V_{IH}	For digital inputs		0.8*V_{CC_H}	-	V_{CC_H}	V
Input logic-low level	V_{IL}			0	-	0.2*V_{CC_H}	V