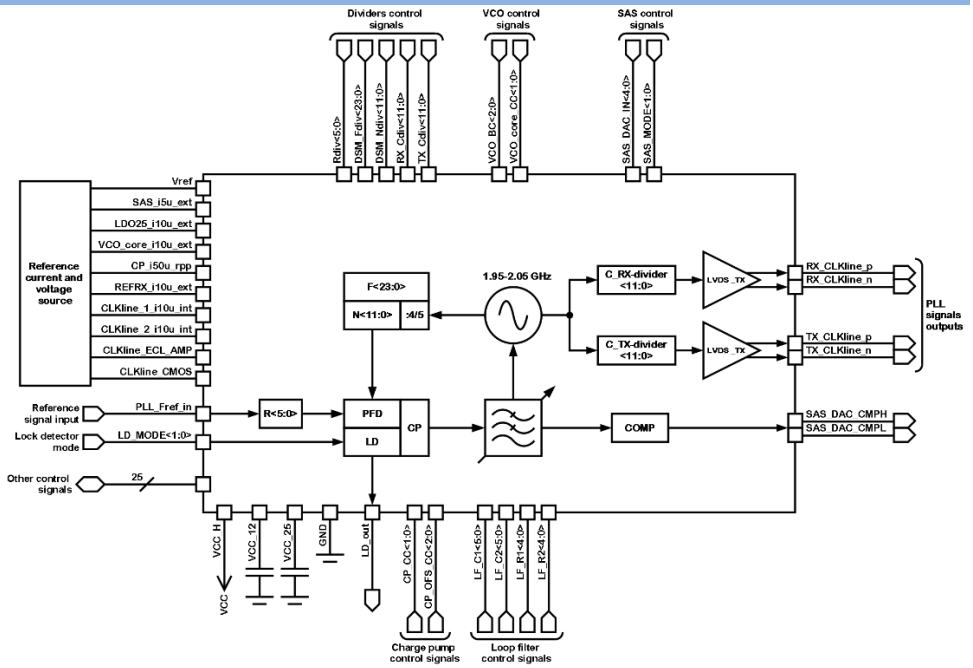
1 to 50MHz phase-locked loop frequency synthesizer

OVERVIEW

055TSMC_PLL_03 is a PLL frequency synthesizer that generates two clock signals in the range from 1 MHz to 50MHz. The synthesizer consists of one voltage-controlled oscillator (VCO) with internal LC circuit and automatic subband selection system; a digital phase frequency detector (PFD); a precision charge pump (CP) with integrated adjustable loop filter; a programmable divider of reference signal; a system of programmable feedback dividers controlled by a delta-sigma modulator (DSM) and output signal dividers.



IP technology: TSMC EF 55 nm technology.
IP status: silicon proven.
Silicon area: 1.053 mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{CC_H}	-	2.25	3.3	3.6	V
	V_{CC25}	-	2.25	2.5	2.75	
	V_{CC12}	-	1.08	1.2	1.32	
Operating temperature range	T_J	-	-40	27	+85	°C
Current consumption in	I_{CC}	-	-	15	-	mA
Reference frequency range	F_{REF}	-	10	-	50	MHz
Output frequency	F_{OUT}	-	1	-	50	MHz
Frequency tuning time	Δt	-	-	-	1.5	ms
C division ratio	C_{DIV}	-	1	-	1023	-
R division ratio	R_{DIV}	-	1	-	32	-
N division ratio	N_{DIV}	-	40		2048	-
Output signal range	$V_{OUT(p-p)}$	-	250	-	400	mV
Output resistance	Z_{OUT}	Differential	-	100	-	Ohm
Input logic-low level	V_{IL}	For digital inputs	0	-	$0.2*V_{CC25}$	V
Input logic-high level	V_{IH}		$0.8*V_{CC25}$	-	V_{CC25}	
Output logic-low level	V_{OL}	For digital outputs	0	-	0.4	V
Output logic-high level	V_{OH}		V_{CC25}-0.4	-	V_{CC25}	