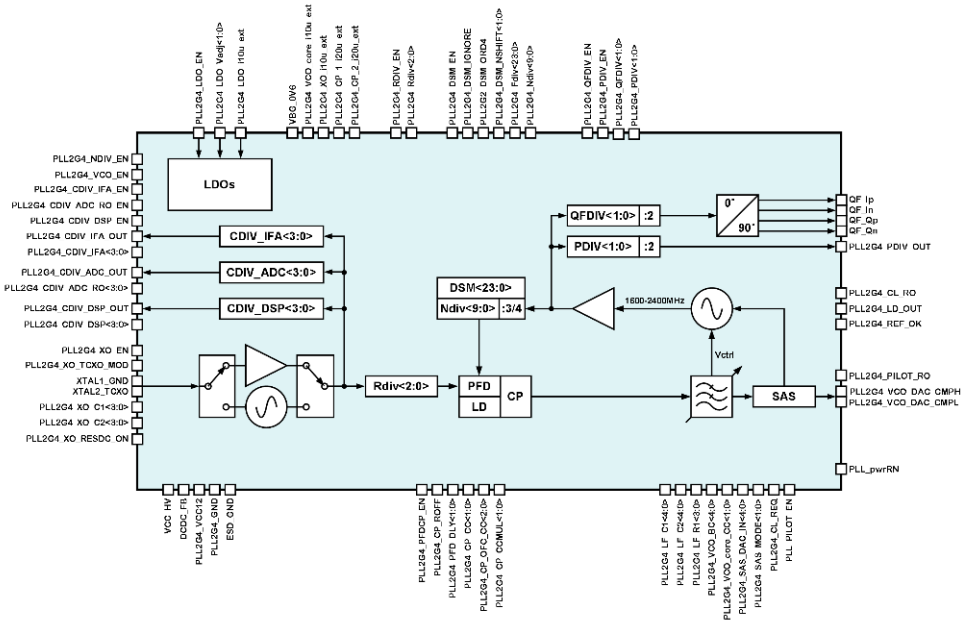
100 - 1200MHz phase-locked loop

OVERVIEW

055TSMC_PLL_08 is a frequency synthesizer with a fractional division ratio and a quadrature output of the heterodyne signal intended for formation, stabilization and frequency modulation (in transmission mode) of the heterodyne signal in the two frequency ranges: 100-150MHz, 200-300MHz, 400-600MHz and 800-1200MHz, as well as for the formation of clock frequency signals from 1.74 to 52MHz. The block is designed to use a 52MHz signal from XTAL or TCXO as a reference frequency.



IP technology: TSMC CMOS 55nm.
IP status: silicon proven.
Silicon area: 1.94mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Unit
Supply voltage	V_{CC_HV}	-		2.25	2.5	2.75	V
	V_{DCDC_FB}	-		1.0	-	1.4	
	V_{CC12}	@PLL2G4_VCC12		1.08	1.2	1.32	
Operating temperature range	T_j	-		-40	+25	+100	°C
Current consumption	I_{DD_RX}	Receiving mode		-	-	2.5	mA
	I_{DD_TX}	Transmission mode		-	-	2.5	
Current consumption in standby mode	I_{std}	-		-	0.5	-	µA
Reference oscillator frequency	F_{ref}	-		-	52	-	MHz
VCO frequency range	F_{VCO}	-		1600	-	2400	MHz
Operating frequency range	F	D1		100	-	150	MHz
		D2		200	-	300	
		D3		400	-	600	
		D4		800	-	1200	
Minimum step of tuning the local oscillator frequency	ΔF	-		-	3	5	Hz
Phase noise spectral density	PN	F = 868MHz	@10kHz	-	-105	-	dBc/Hz
			@100kHz	-	-110	-	
			@1MHz	-	-123	-	
Jitter value	J_{RMS}	F = 868MHz		-	717	-	fs
Input logic-high level	V_{IH}	-		0.8*V_{CC12}	-	V_{CC12}	V
Input logic-low level	V_{IL}	-		0	-	0.4	
Output logic-high level	V_{OH}	-		V_{CC12} – 0.4	-	V_{CC12}	
Output logic-low level	V_{OL}	-		0	-	0.4	