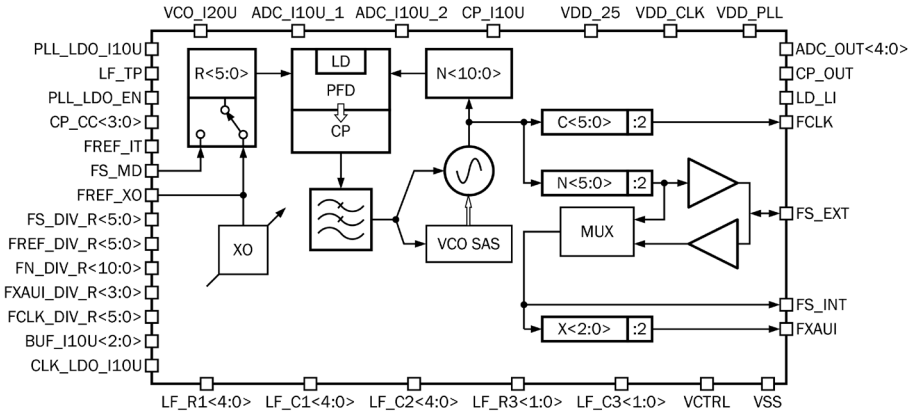
12 – 750 MHz phase-locked loop clock generator

OVERVIEW



065TSMC_PLL_07 is an integer-N phase-locked loop frequency synthesizer (PLL) based on fully integrated 2 GHz LC-VCO with low gain and fine phase noise performance. It works with reference frequency from 25MHz XTAL oscillator or external signal source with frequency up to 500MHz. Phase-frequency divider compare frequency can be equal or 1,2,3...31 times lower than reference. VCO frequency N-divider has programmable coefficient of division with step 1 in range 4 to 2047. Phase-frequency detector has built-in analog and digital lock detector circuits. Charge pump scheme with ADC and adjustable output current allow compensation VCO gain variation within band and keep loop gain constant. Integrated low-pass loop filter has adjustable values of resistance and capacitance for tune loop and get best phase-noise performance. All of output clocks have 0.5 duty cycle value using duty cycle recovery circuit.

IP technology: TSMC CMOS 65nm.

IP status: silicon proven.

Area: 0.95mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition		Value			Units
				min	typ.	max	
Supply voltage	V_{DD_25}	-		2.375	2.5	2.625	V
VCO control voltage	V_{CTRL}	-		0.5	-	2.0	V
Internal regulated supply voltage	V_{DD_PLL}	-		1.14	1.2	1.29	V
Temperature range	T_j	-		-40	85	125	°C
VCO frequency range	F_{vco}	Typical case		1850	-	2140	MHz
Internal reference frequency	F_{ref_int}	-		-	25	-	MHz
External reference frequency	F_{ref_ext}	-		25	-	500	MHz
Phase-detector frequency	F_{pfd}	-		-	-	250	MHz
Phase noise	PN	F_S = 500MHz	@10kHz	-	-97	-	dB/Hz
			@100kHz	-	-99	-	
			@1MHz	-	-124	-	
			@10MHz	-	-135	-	
Period jitter (rms)	J	F_S = 500MHz		-	2	-	ps
Charge pump sink/source current value	I_{CP}	-		20	-	320	uA
Standby current	I_{st}	Without input signal		-	<1	-	uA
Internal loop filter R1 value	R1	-		5	-	82.5	kOhm
Internal loop filter C1 value	C1	-		24	-	768	pF
Internal loop filter C2 value	C2	-		3	-	96	pF
Fs frequency value	F_S	Full voltage swing 45..55% duty cycle		107	-	750	MHz
Fxaui frequency value	F_{XAUI}			50	-	750	MHz
Fclk frequency value	F_{CLK}	Reduced voltage swing 45..55% duty cycle		12	-	750	MHz
Reference frequeny divider ratio	R_{div}	-		1	-	31	-
VCO frequency divider ratio	N_{div}	-		4	-	2047	-
Input logic-high level	V_{IH}	For digital inputs		0.8*V_{DD_25}	-	V_{DD_25}	V
Input logic-low level	V_{IL}			0	-	0.2	V