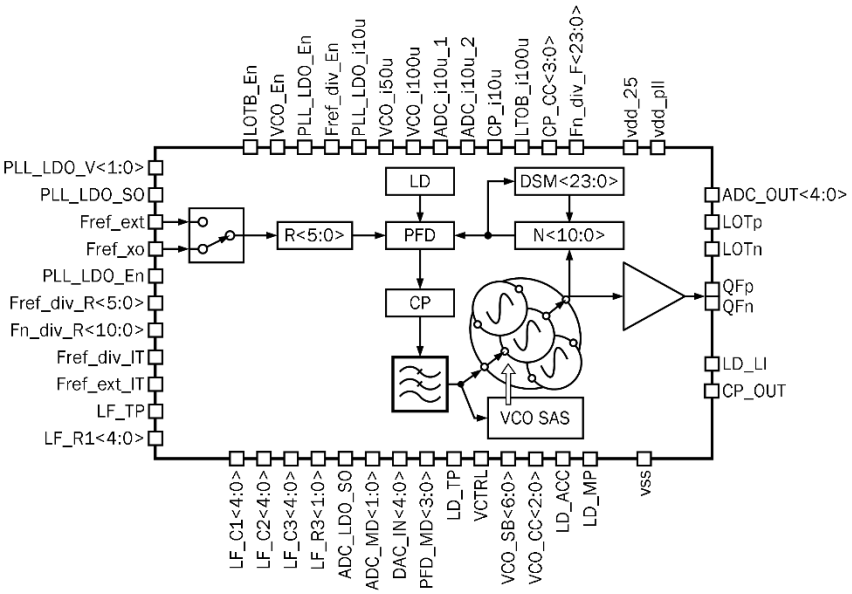
Wide band 3Ghz-6GHz fractional phase-locked loop

OVERVIEW

065TSMC_PLL_09 is a phase-locked loop frequency synthesizer with integer-N/fractional-N modes based on fully integrated wide band LC-VCO with range from 3GHz to 6GHz with good phase noise performance. It works with reference frequency from 5MHz to 50MHz or external signal source with frequency up to 500MHz. Phase-frequency divider compare frequency can be equal or 2,3,4...63 times lower than reference. VCO frequency N-divider has programmable coefficient of division with step 1 in range 4 to 2047 modulated with 4-order 24bit DSM. Phase-frequency detector has built-in lock detector circuit. Charge pump scheme with ADC and adjustable output current allow compensation VCO gain variation within band and keep loop parameters constant. Integrated low-pass loop filter has adjustable values of resistance and capacitance for tune loop and get best phase-noise performance.



IP technology: TSMC CMOS CRN65LP.
IP status: silicon proven. Area: 1.1mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{dd_25}	-		2.4	2.5	2.6	V
	V_{dd_pll}	-		1.14	1.2	1.26	
Operating temperature range	Tj	-		-40	+85	+125	°C
VCO control voltage	V_{ctrl}	-		0.5	-	2.0	V
VCO frequency range	F_{vco}	VCO 1		2630	-	4090	MHz
		VCO 2		3520	-	5450	
		VCO 3		4850	-	6810	
VCO gain	K_{vco}	-		25	90	230	MHz/V
Open loop VCO phase noise performance	PN_{VCO}	V_{dd_pll} = 1.24V, F_{LO} = 2GHz	@10kHz	-	-93	-	dBc/Hz
			@100kHz	-	-98	-	
			@1MHz	-	-114	-	
Period jitter (rms)	J	V_{dd_pll} = 1.24V, F_{LO} = 2GHz		-	1.1	-	ps
LO frequency range	F_{LO}	-		75	-	3000	MHz
Step of tuning LO frequency	ΔF_{LO}	-		-	25	-	MHz
Internal reference frequency	F_{ref_int}	-		5	25	50	MHz
External reference frequency	F_{ref_ext}	-		25	-	500	MHz
PFD frequency	F_{PFD}	-		-	-	250	MHz
Internal loop filter R1 value	R1	-		5	-	82.5	kOhm
Internal loop filter C1 value	C1	-		24	-	768	pF
Internal loop filter C2 value	C2	-		3	-	96	pF
Reference frequency spurious suppression	SS_{rf}	-		-	70	-	dB
Reference frequency divider ratio	Rdiv	-		1	-	63	-
VCO frequency divider ratio	Ndiv	-		4	-	2047	-
Current consumption without output buffer	I_{CC}	-		-	9.5	-	mA
Standby current	I_{sb}	Without input signal		-	<1	-	uA
Input logic high level	V_{IH}	For digital inputs		0.8*V_{dd_25}	-	V_{dd_25}	V
Input logic low level	V_{IL}			-0.2	-	+0.2	V