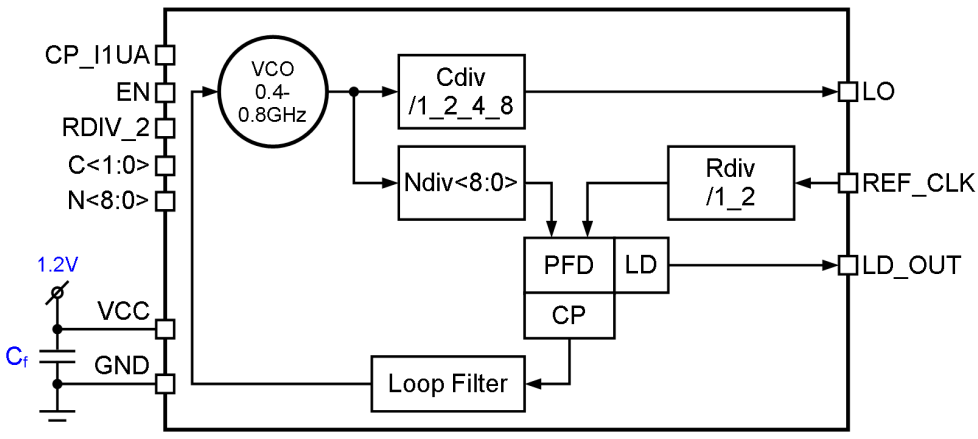
50MHz to 800MHz Integer-N Phase-Locked Loop

OVERVIEW

065TSMC_PLL_10 is a integer-N synthesizer, which forms clock signal with frequency from 50 to 800 MHz. It consists of the ring VCO with frequency from 400 to 800 MHz, a programmable feedback divider, a low noise digital phase noise detector (PFD), a precision charge pump (CP) with internal loop filter, lock detector (LD) and programmable clock divider to obtain a required output frequency. Output frequency is calculated by formula: $F_{LO} = (F_{ref}*N)/(R*C)$. Output signal is CMOS compatible.



IP technology: TSMC CMOS 65 nm.
IP status: silicon proven.
Area: 0.0088mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{CC}	-	1.1	1.2	1.3	V
Operating temperature range	T_j	-	-40	27	85	ºC
Output frequency	F_{out}	-	50	-	800	MHz
LO duty cycle	LO_{DC}	-	40	50	60	%
Phase noise	LO_{PN}	at 1 MHz	-	-97	-	dBc/Hz
Reference current	I_{ref}	Source from power	0.72	0.85	1.0	uA
Reference frequency	F_{ref}	-	4	6	30	MHz
Ref_clk duty cycle	Ref_clk_{DC}	-	40	50	60	%
VCO control voltage	V_{ctrl}	-	0.2	-	1.0	V
Comparison frequency	F_{comp}	-	4	-	15	MHz
Lock time	T_{lock}	-	-	17	30	us
Lock detector accuracy	S_{err}	-	15	20	25	ns
Lock detector frequency accuracy	F_{err}	-	10	12	16	MHz
Lock monitoring period	MP	$T_{comp} = 1/F_{comp}$	-	$32*T_{comp}$	-	us
Current consumption	I_{cc}	F_{out} = 400 MHz	160	210	250	uA
		F_{out} = 800 MHz	350	410	450	
Current consumption in standby mode	I_{stb}	-	-	0.03	2.7	uA
Reference signal - high level	V_{RefH}	CMOS	$0.8V_{cc}$	-	1.3	V
Reference signal - low level	V_{RefL}		-0.1	-	0.2	
Input logic - high level	V_{IH}	For digital inputs	$0.8V_{cc}$	-	1.3	V
Input logic - low level	V_{IL}		-0.1	-	0.2	