Phase-locked loop frequency synthesizer

SPECIFICATION

1 FEATURES

- CMOS UMC 65 nm
- Integer-N frequency synthesizer with good phase noise performance
- Guaranteed frequency range 550…750 MHz
- Wide continuous loop frequency divider ratio range (16..2047 with step 1) allow to cover frequency range using different reference frequency
- Wide continuous reference frequency divider ratio range (1..31 with step 1) allow to use high reference frequency or reach high frequency resolution
- Integrated lock detector circuit with high accuracy
- Integrated loop filter with adjustment ability
- No external components required
- Low power consumption
- Portable to other technologies (upon request)

2 APPLICATION

- Portable transmitters and transceivers

3 FUNCTIONAL DESCRIPTION

PLL is an automatic control system adjusting controlled oscillator frequency to be equal to reference oscillator frequency multiplied by a given integer ratio. Frequency adjustment is carried out by using negative feedback. A phase detector compares a controlled oscillator output with a reference signal. The result is a charge pump current output that supplies feedback low-pass filter and converted to a voltage for controlled oscillator adjustment.
Clock divider is used to generate signals with specified frequency.
This block designed for CMOS UMC 65 nm technology.

4 STRUCTURE

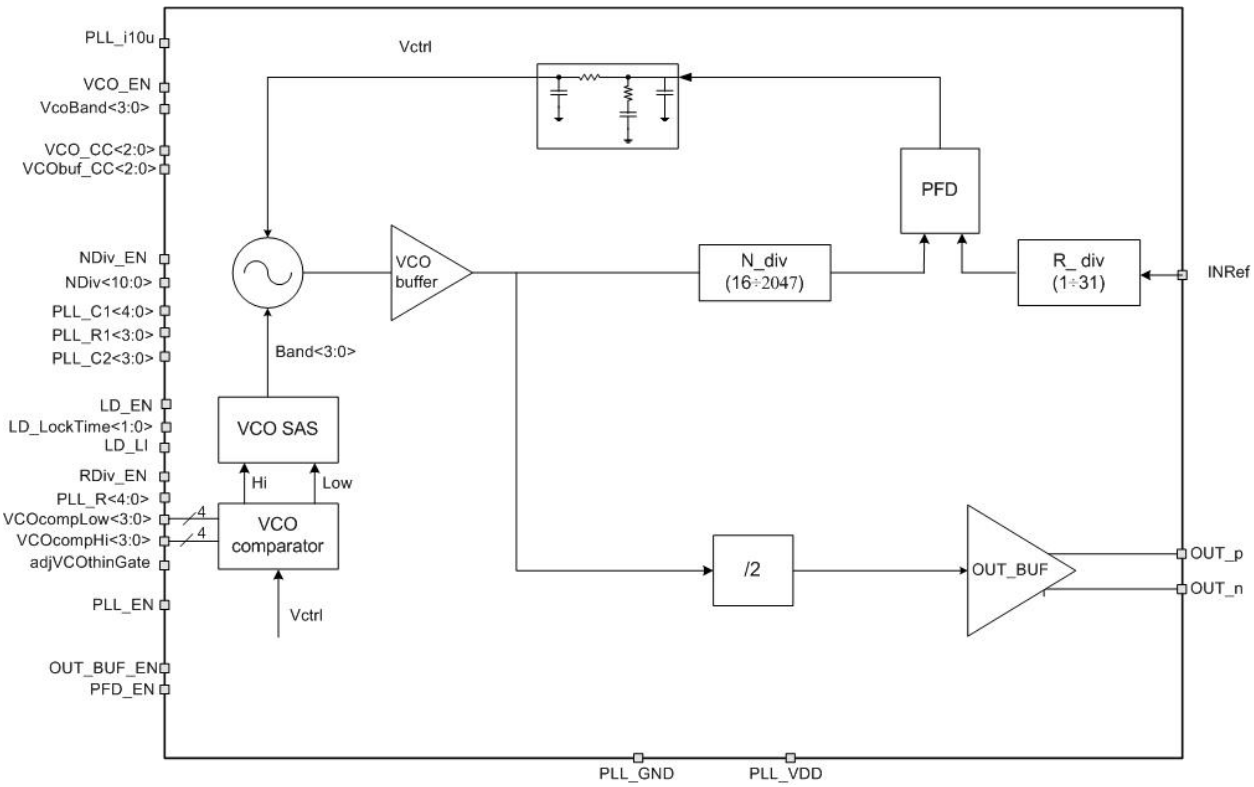

Figure 1: Phase-locked loop frequency synthesizer structure.

5 PIN DESCRIPTION

Name	Direction	Description
PLL_i10u	I	Reference current 10µA
VCO_EN	I	VCO enable/disable
PFD_EN	I	Phase-frequency detector enable/disable
PLL_EN	I	PLL enable/disable
RDiv_EN	I	Reference frequency divider enable/disable
Ndiv_EN	I	VCO frequency divider enable/disable
LD_EN	I	Lock detector enable/disable
OUT_BUF_EN	I	Output buffer enable/disable
VCO_CC<2:0>	I	VCO core current selection
VCO_BUF_CC<2:0>	I	Buffer current selection
CP_CC<1:0>	I	Charge pump output current control
VcoBand<3:0>	I	Switching capacitor sections (VCO subbands)
NDiv<10:0>	I	Dividing ratio of VCO frequency divider
PLL_R<4:0>	I	Dividing ratio of reference frequency divider
LD_LockTime<1:0>	I	Lock detector monitoring period selection
adjVCOthinGate	I	Fixed/programmable bounds mode control
VCOcompHi<3:0>	I	Upper bound voltage selection for VCO subband autoselect system
VCOcompLow<3:0>	I	Lower bound voltage selection for VCO subband autoselect system
INref	I	Reference frequency input
PLL_C1<4:0>	I	PLL loop filter adjust
PLL_C2<3:0>	I	
PLL_R1<3:0>	I	
LD_LI	O	Lock indicator
OUT_n	O	Differential clock output
OUT_p	O	
VDD	IO	Supply voltage
GND	IO	Ground

LAYOUY DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	1160	µm
Width	600	µm

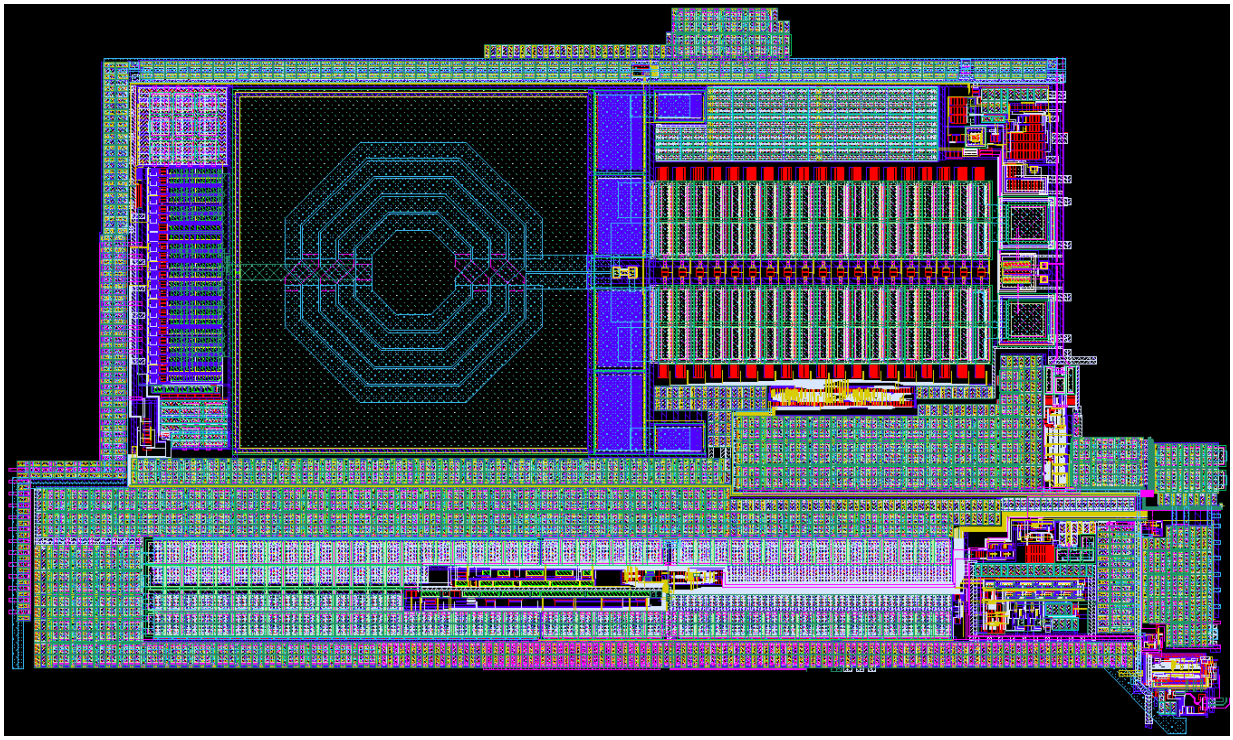

Figure 2: Phase-locked loop frequency synthesizer layout view.

6 OPERATING CHARACTERISTICS

6.1 TECHNICAL CHARACTERISTICS

Technology _____ UMC CMOS 65 nm
Status _____ silicon proven
Area _____ 0.7 mm^2

6.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.4 ÷ 2.6 V and T = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.5 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	2.4	2.5	2.6	V
Operating temperature range	T	-	-45	27	85	°C
PLL dividing ratio	N_{PLL}	-	16	-	2047	-
Reference frequency	F_r	-	1	-	50	MHz
Output frequency range	F_{OUT}	-	550	-	750	MHz
Peak-to-peak output voltage	A_{OUT}	Differential output	0.4	0.6	0.8	V
Reference frequency divider ratio	R_{PLL}	-	1	-	31	-
Comparison frequency range	F_{PFD}	-	0.1	-	50	MHz
Lock accuracy	LD_Acc	Preset 1	6	7	8	ns
Current consumption in an active mode	I_{cc}	-	2.8	3	3.2	mA
Current consumption in a standby mode	I_{stb}	-	-	-	1	uA
Oscillator phase noise spectral concentration	PN	at 100kHz offset	-	-	-100	dBc/Hz
Input logic-high level	V_{IH}	For digital inputs	0.9 V_{cc}	-	1.2	V
Input logic-low level	V_{IL}		-0.1	-	0.1	V

7 DELIVERABLES

IP contents include:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optinal)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optinal)
- Documentation