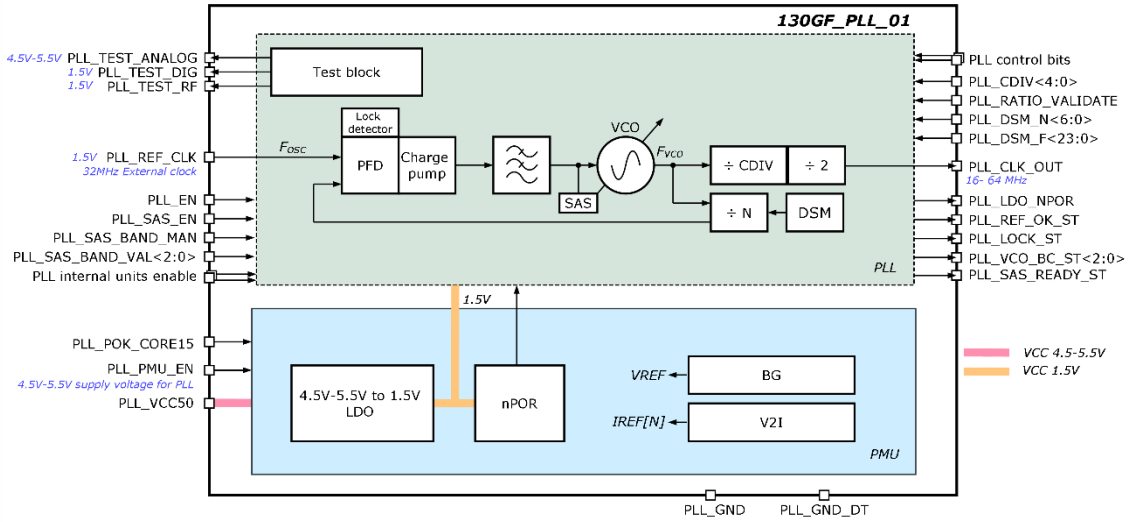
16 to 64 MHz Phase-Locked Loop

OVERVIEW



130GF_PLL_01 is a ring VCO based phase-locked loop frequency with 16-64 MHz CMOS compatible output clock and fine frequency resolution thanks to the embedded delta-sigma modulator (DSM). The IP consists of a ring voltage controlled oscillator (VCO) with multiple sub-bands and sub-band autoselection system (SAS), a programmable N feedback divider (÷N) controlled by DSM, a digital phase-frequency detector (PFD) with a lock detector (LD), a charge pump (CP) with internal loop filter, a power management unit (PMU), and a programmable C clock divider (÷C).

IP technology: GF BCD 130 nm technology

IP status: silicon proven

Area: 0.2 mm^2

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
IO supply voltage	PLL_VCC50	External source	4.5	5.0	5.5	V
PLL supply voltage	VCC15	Internal LDO	1.42	1.50	1.53	V
Operating temperature range	Tj	-	-40	+25	+125	°C
Current consumption		PLL is operating and is in lock	-	0.65	1	mA
		Stand-by	-	10	220	nA
Input frequency	F_{IN}	-	-	32	-	MHz
VCO frequency range (guaranteed)	F_{VCO}	-	640	-	770	MHz
VCO phase noise	PN_{VCO}	@10kHz	-	40	-	dB
		@100kHz	-	69	-	
		@1MHz	-	95	-	
		@10MHz	-	116	-	
N divider ratio	N	-	9	-	63	-
F divider ratio	F	-	0	-	16777215	-
Frequency resolution	Res	-	-	0.2	-	Hz
Output clock RMS jitter	$J_{RMS\_PLL\_CLK}$	1kHz–10MHz	-	-	35	ps
Start-up time	T_{PLL}	with executing sub-band autoselection	-	450	500	µs
		without executing sub-band autoselection	-	150	200	µs