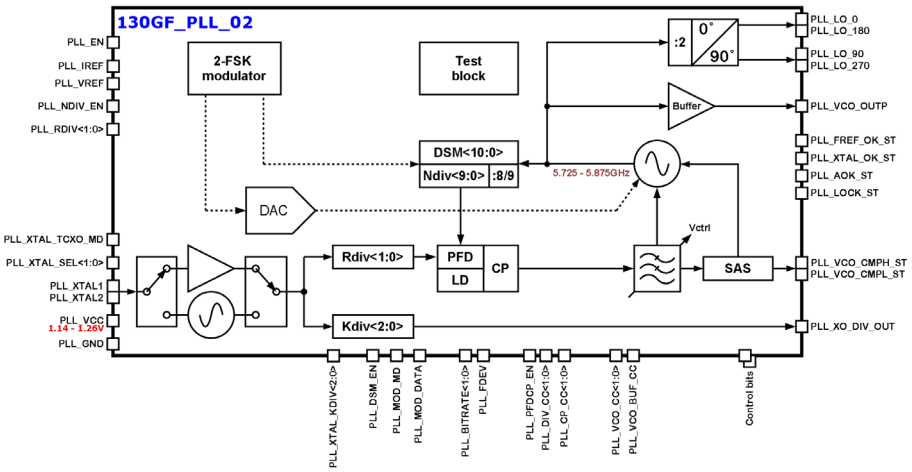
5.8GHz Fractional-N PLL synthesizer

OVERVIEW

130GF_PLL_02 is intended for SoC clock generation with support of BFSK modulation up to 4Mbps output data rate. PLL IP block embeds a reference 8MHz/16MHz/ 32MHz/64MHz XTAL oscillator, which is able to work as an input signal buffer in the same frequency range.

The internal 5.725GHz-5.875GHz high frequency VCO provides both excellent phase noise performance and ultra-fine frequency tuning step.



Quadrature former is intended to generate differential output signals with phase shift 90°, coherent to input signal.

IP technology: GF 130nm CSOI.

IP status: pre-silicon verification.

Area: 1.98mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{PLL_VCC}	–		1.14	1.2	1.26	V
Operating temperature range	T_j	–		0	+50	+100	°C
Current consumption	I_{CC}	@RX mode		-	23.8	-	mA
		@TX mode		-	19.8	-	
XTAL frequency	Fref	-		16	-	64	MHz
Operating frequency range	F_{VCO}	-		5.725	-	5.875	GHz
Output clock frequency range	F_{KDIV}	PLL_XO_DIV_OUT, adjustable		-	0.5	-	MHz
				-	1	-	
				-	2	-	
				-	4	-	
				-	8	-	
				-	16	-	
Buffer output frequency range	F_{out}	@TX mode, PLL_VCO_OUTP		5.725	-	5.875	GHz
		Sine wave, high-Z load		-20	-	-10	dBm
Transmission bit rates	BR	Adjustable		-	0.5	-	Mbps
				-	1	-	
				-	2	-	
				-	4	-	
Phase noise (1MHz loop BW).		TX mode: F = 5.8GHz, Fref = 32MHz, data rate 4Mbps	@10kHz	-	-89.4	-	dBc/Hz
			@100kHz	-	-90.7	-	
			@1MHz	-	-90.7	-	
			@10MHz	-	-98.8	-	
QF output frequency range	F_{out_QF}	@RX mode, PLL_LO_* outputs		2.8625	-	2.9375	GHz
Phase noise (120kHz loop BW).		RX mode: F = 5.8GHz, Fref = 32MHz	@10kHz	-	-95.1	-	dBc/Hz
			@100kHz	-	-94.2	-	
			@1MHz	-	-120.7	-	
			@10MHz	-	-134.9	-	
		RX mode, F_{VCO} = 5.8GHz, Fref = 32MHz		-	0.8	1.2	ps