

Frequency synthesizer 20÷300MHz

DESCRIPTION

1 FEATURES

- SilTerra CMOS18G
- Reference signal frequency from 8 to 16 MHz
- Output frequency from 20 to 300 MHz
- Power supply 1.8V
- Temperature range -40...125 °C
- Current consumption less than 2mA
- Size 300x300 um
- Portable to other technologies (upon request)

2 APPLICATION

- Data receiving/transmitting systems
- Clock signal generator
- Testing equipment

3 OVERVIEW

The system generates stable clock signal with frequency from 20 to 300 MHz. The synthesizer is based on an integer Phase Locked Loop (PLL).

Input ckref is connected to reference clock signal with frequency from 8 to 16 MHz. Output pll_clk is signal with desired frequency.

4 STRUCTURE

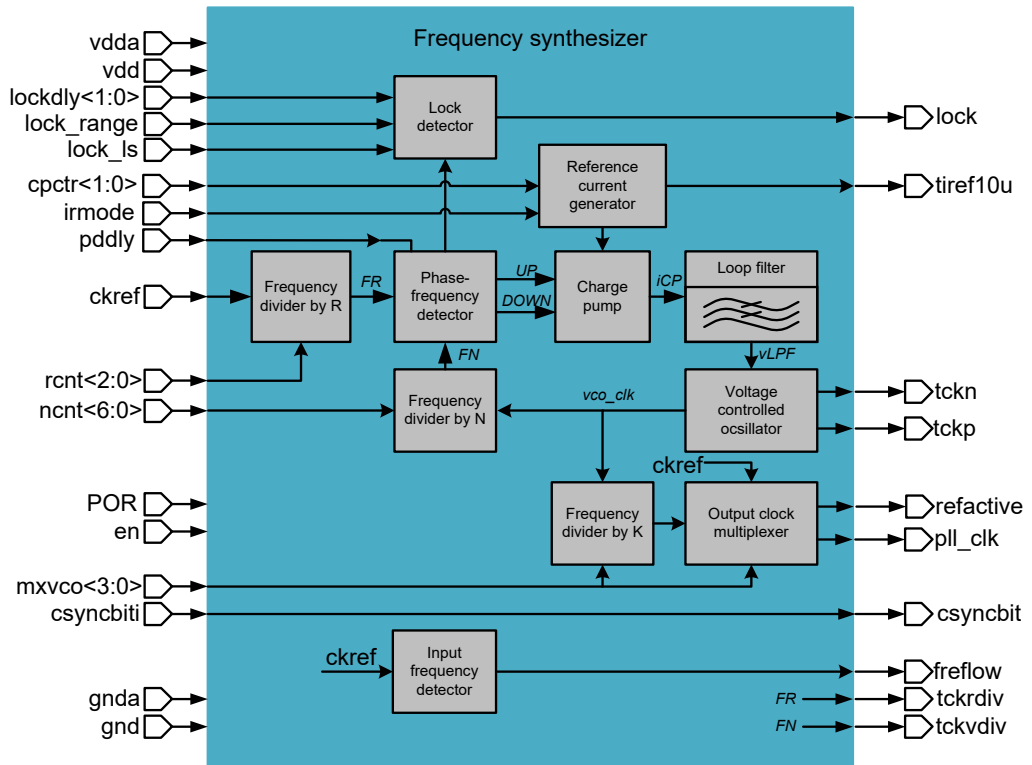


Figure 1: Block structure of the frequency synthesizer.

5 PIN DESCRIPTION

Name	Direction	Description
tiref10u	IO	Test output of internal 10uA current reference
ckref	I	Input reference frequency clock
rcnt<2:0>	I	Control bits of R divider
ncnt<6:0>	I	Control bits of N divider
mxvco<3:0>	I	Control bits of output multiplexer with K-divider
POR	I	Reset
en	I	Enable
pddly	I	Control bit of PFD reset time
cpctr<1:0>	I	Control bits of charge pump
irmode	I	Control bit of reference current
lockdly<1:0>	I	Control bits of lock detector
lock_range	I	Control bits of lock detector
lock_ls	I	Control bits of lock detector
csyncbiti	I	Test input bit
pll_clk	O	Output synthesized clock
reflow	O	Indication of low reference frequency
lock	O	Indiction of stable clock generation
refactive	O	Indication that pll_clk is reference clock
tckn	O	Test output from VCO
tckp	O	Test output from VCO
tckrdiv	O	Test output from R divider
tckvdiv	O	Test output from N divider
csyncbit	O	Buffered signal of csyncbiti
vdda	IO	Analog supply 1.8V
gnda	IO	Analog ground
vdd	IO	Digital supply 1.8V
gnd	IO	Digital ground

6 LAYOUT DESCRIPTION

Table 1: Dimensions of IP layout

Dimension	Value	Unit
Height	299	um
Width	283	um

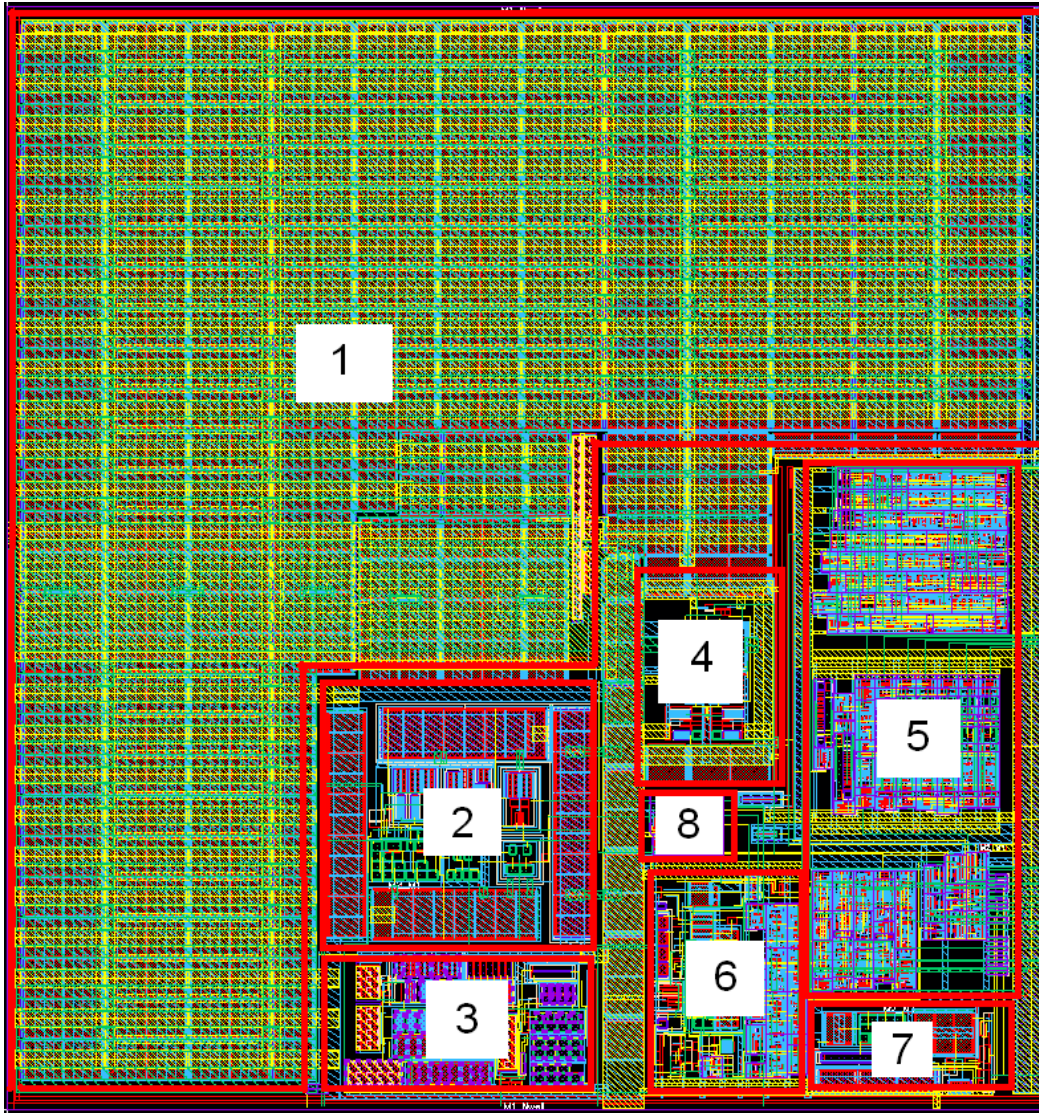


Figure 2: Frequency synthesizer layout.

- 1 Loop filter
- 2 Charge pump
- 3 Current reference
- 4 VCO
- 5 Dividers and output multiplexer
- 6 Lock detector
- 7 Reference clock low frequency detector

7 OPERATION CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ SilTerra CMOS 0.18um
 Status _____ pre-silicon verification
 Area _____ 0.09 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical parameters are specified for $V_{dd}=1.6 \div 2.0$ V, $V_{dda}=1.6 \div 2.0$ V and $T_j = -40 \div +125^\circ\text{C}$, unless otherwise noted. Typical values are given for $V_{dd}=1.8$ V, $V_{dda}=1.8$ V and $T_j = +27^\circ\text{C}$.

Parameter name	Symbol	Conditions	Value			Unit
			min	typ	max	
Junction temperature range	T_j	-	-40	27	125	$^\circ\text{C}$
Digital supply	V_{dd}	-	1.6	1.8	2	V
Analog supply	V_{dda}	-	1.6	1.8	2	V
Supplies difference	$V_{dda}-V_{dd}$	-	-0.1	0	0.1	V
Current consumption	I_{cn}	$F_{pll_clk} < 300$ MHz	-	-	2	mA
		$F_{pll_clk} > 300$ MHz	-	-	4	
Standby current	I_{st}	-	-	-	10	μA
Dissipated power	W_{dd}	-	-	-	4	mW
Reference clock frequency	F_{ckref}	-	8	-	16	MHz
Output clock frequency	F_{pll_clk}	-	20	-	300	MHz
Frequency step	dF_{pll_clk}	-	1	-	16	MHz
Setting time	T_{sw}	-	-	-	1	ms
Output clock duty cycle	D_{clk}	-	43	-	57	%
Period jitter (peak-to-peak)	J_{pll_clk}	$F_{pll_clk} = 300$ MHz	-	-	400	ps
Input logic-level high	V_{IH}	For digital	$V_{dd}-0.2$	-	2	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DYNAMIC CHARACTERISTICS

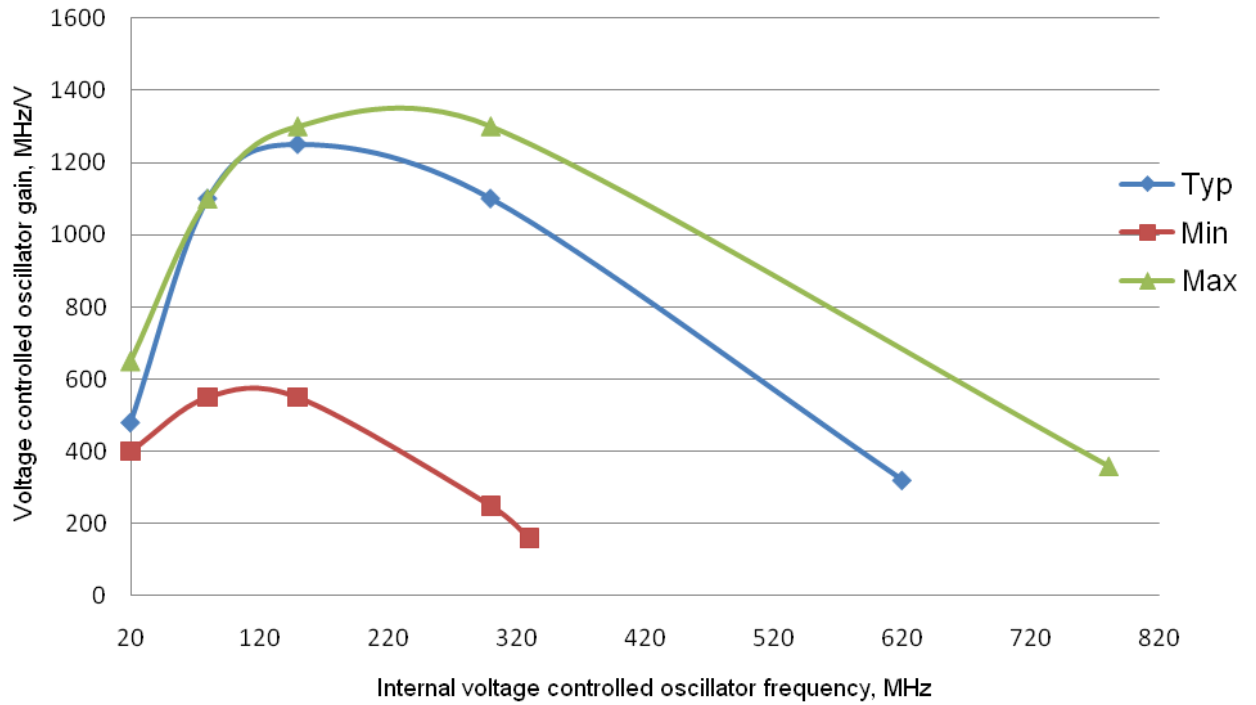


Figure 3: VCO gain dependence on VCO frequency.

9 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation