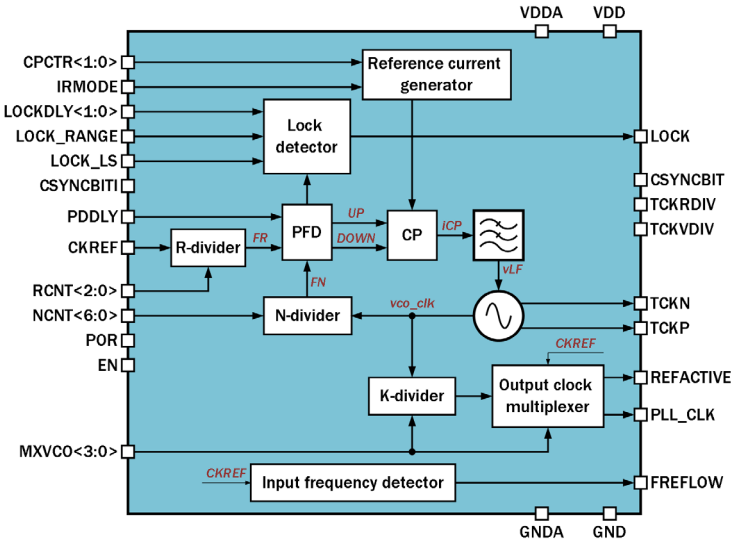
20 to 300 MHz integer-N frequency synthesizer

OVERVIEW

180SIL_PLL_01 is an integer-N PLL frequency synthesizer that generates a 20MHz to 300MHz output clock. The IP block uses 8MHz to 16MHz reference clock at **CKREF**. Build-in reference frequency detector indicates when reference frequency is too low.

IP technology: SilTerra CMOS18G.
IP status: silicon proven.
Area: 0.085mm^2.



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Digital supply voltage	V_{DD}	-	1.6	1.8	2.0	V
Analog supply voltage	V_{DDA}	-	1.6	1.8	2.0	V
Supplies difference	ΔV_{DD}	$V_{DDA} - V_{DD}$	-0.1	0	0.1	V
Operating temperature range	T_j	-	-40	+27	+125	°C
Reference clock frequency	F_{CKREF}	-	8	-	16	MHz
Output clock frequency	F_{PLL_CLK}	-	20	-	300	MHz
Frequency step	ΔF_{PLL_CLK}	-	1	-	16	MHz
Settling time	T_{sw}	-	-	-	1	ms
Output clock duty cycle	D_{PLL_CLK}	-	43	-	57	%
Period jitter (peak-to-peak)	J_{PLL_CLk}	$\pm 3\sigma @ F_{pll\_clk} = 300MHz$	-	-	400	ps
Current consumption	I_{CC}	-	-	-	2	mA
Standby current	I_{st}	-	-	-	3	uA
Input logic-level high	V_{IH}	For digital inputs	V_{DD}-0.2	-	2	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V