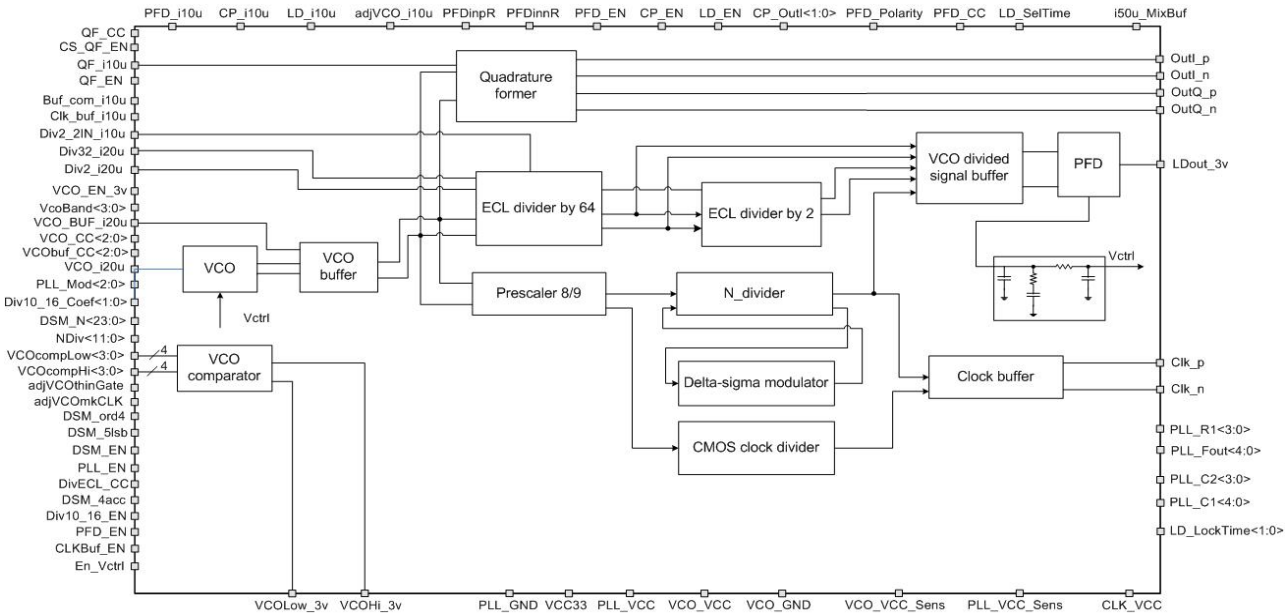
2.8 to 3.3 GHz phase-locked loop system

OVERVIEW



180SMIC_PLL_02 is an automatic control system adjusting controlled oscillator frequency to be equal to reference oscillator frequency multiplied by a given integer. Frequency adjustment is carried out by using negative feedback. A phase detector compares a controlled oscillator output with a reference signal. The result is a charge pump current output that supplies external feedback filter and converted to a voltage for controlled oscillator adjustment. Clock divider is used to generate signals with specified frequency. Delta-sigma modulator makes it possible to operate with reference oscillator of different frequency.

IP technology: SMIC CMOS 180nm.

IP status: silicon proven.

Area: 0.67mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Units
			min	typ.	max	
Supply voltage	V_{cc33}	-	2.7	3.3	3.6	V
	V_{VCO_VCC}	-	1.7	1.8	1.9	
	V_{PLL_VCC}	-	1.7	1.8	1.9	
Operating temperature range	Ta	-	-45	27	85	°C
Current consumption	I_{cc}	Active mode	4.3	5.9	7.5	mA
	I_{stb}	Standby mode	-	70	-	nA
VCO frequency range	F_{VCO}	-	2.8	-	3.3	GHz
Peak-to-peak output voltage	A_{VCO}	Differential output	740	-	-	mV
Reference frequency	F_r	-	-	24.84	-	MHz
Output clock frequency	F_{clk}	-	-	49.68	-	MHz
Quadrature former frequency	F_{QF}	-	2.8	-	3.3	GHz
Peak-to-peak at clock frequency differential outputs (Fclk)	A_{cmos}	CMOS	1.7	1.8	1.9	V
		Differential output	0.3	0.32	0.45	
PLL dividing ratio	N_{PLL}	-	56	-	16383	-
R divider programmable values	R_{PLL}	-	1	-	32	-
Comparison frequency range	F_{PFD}	-	-	24.84	-	MHz
Lock monitoring time	Sel_time	-	2.58	-	20.6	us
Lock accuracy	Prec_lock	Preset 1	6.5	7	7.5	ns
		Preset 2	13	14	15	
PLL phase noise spectral concentration	PN_{PLL}	@10kHz offset	-	-83	-80	dBHz
Input logic-high level	V_{IH}	For digital inputs	0.7*V_{PLL_VCC}	-	3.6	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V