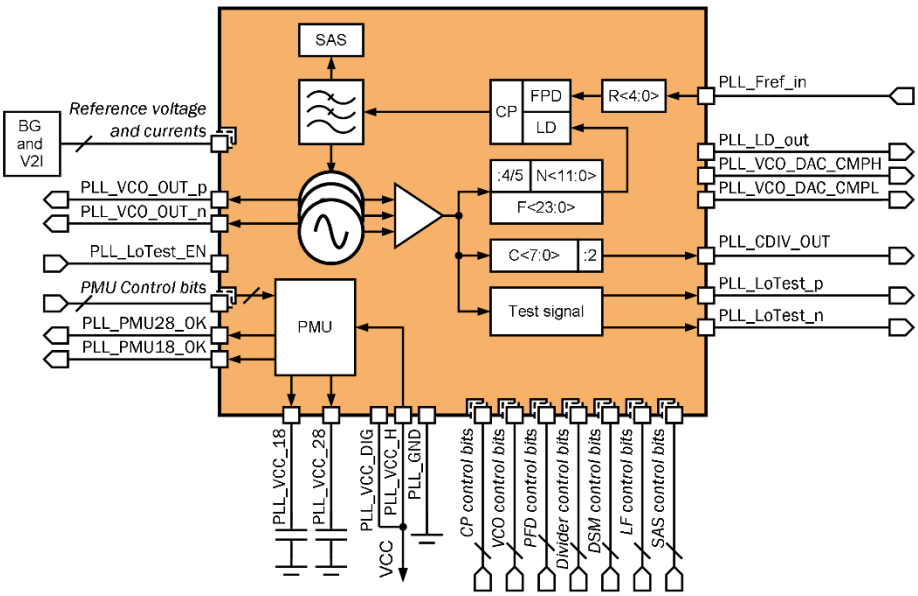
1GHz to 3GHz, 6MHz to 100MHz Fractional-N Phase-Locked Loop

OVERVIEW

180TSMC_PLL_10 is designed to generate a high frequency signal in a range from 1GHz to 3GHz and a low frequency clock signal in a range from 6MHz to 100MHz. The frequency synthesizer consists of a voltage controlled oscillator (VCO) with an internal LC-circuit; system of programmable feedback dividers; digital frequency-phase detector (FPD); precision charge pumping system (CP) with built-in loop filter; programmable frequency divider of the reference signal; delta-sigma modulator (DSM); a system of comparators for automatic selection of the VCO subrange and power management unit (PMU). The PMU performs the function of a voltage regulator with the ability to select the maximum output voltage for indicating increased current consumption.



IP technology: TSMC SiGe BiCMOS 180nm.
IP status: silicon proven.
Area: 2.278mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions		Value min	Value typ.	Value max	Units
Supply voltage	V_{CC}	-		2.97	3.3	3.63	V
Temperature range	T_J	-		-40	+25	+100	°C
Current consumption	I_{CC}	-		-	11.7	-	mA
Stand-by current	I_{STB}	@PMU enabled		-	0.13	-	mA
Output frequency range	F_{VCO}	VCO1		1	-	1.4	GHz
		VCO2		1.4	-	2.1	
		VCO3		2.1	-	3	
Output VCO frequency	F_{VCO}	@PLL_VCO_OUT_p and PLL_VCO_OUT_n		1	-	3	GHz
Peak-to-peak differential VCO output	$V_{p\text{-}pVCO}$	-		-	0.6	-	V
Output frequency step	ΔF	-		100	-	-	kHz
Output frequency setting time	Δt	-		-	-	5	ms
Reference input frequency	F_{REF}	-		10	-	50	MHz
Clock output frequency	F_{CLK}	@PLL_CDIV_OUT		6	-	100	MHz
Output clock duty cycle	D_{CLK}	-		-	50	-	%
Clock output peak-to-peak voltage	ΔV_{CLK}	CMOS		V_{CC}-0.1	-	-	V
Phase noise	PN	@1MHz	F_{VCO} = 1GHz	-	-124.7	-	dB/Hz
			F_{VCO} = 2GHz	-	-120.7	-	
			F_{VCO} = 3GHz	-	-118.4	-	
Jitter value	J_{VCO}			-	0.8	-	ps
Reference frequency division factor	R	-		1	-	31	-
N divider ratio	N	-		16	-	4095	-
C divider ratio	C	With step 2		8	-	510	-