Phase-locked loop frequency synthesizer

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide frequency range (120 to 950 MHz)
- Operating frequency selection using external components
- Built-in switched capacitor sections for VCO frequency adjustment
- Low noise figure
- High lock detector accuracy
- Charge pump low output current disbalance
- Built-in reference frequency oscillator
- Programmable clock frequency divider
- Small area
- Low current consumption
- Low power consumption
- Portable to other technologies (upon request)

2 APPLICATION

- Portable transmitters
- Portable transceiver

3 OVERVIEW

The PLL is an automatic control system which can be used to implement local oscillators (LO) in wireless receivers and transmitters. This device consists of a voltage controlled oscillator (VCO) with external LC tanks, programmable feedback dividers, a low noise digital phase noise detector (PFD), a precision charge pump (CP) with external loop filter, a quartz oscillator with external quartz resonator, programmable reference dividers, comparators of a VCO subband autoselect system and two voltage regulators.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

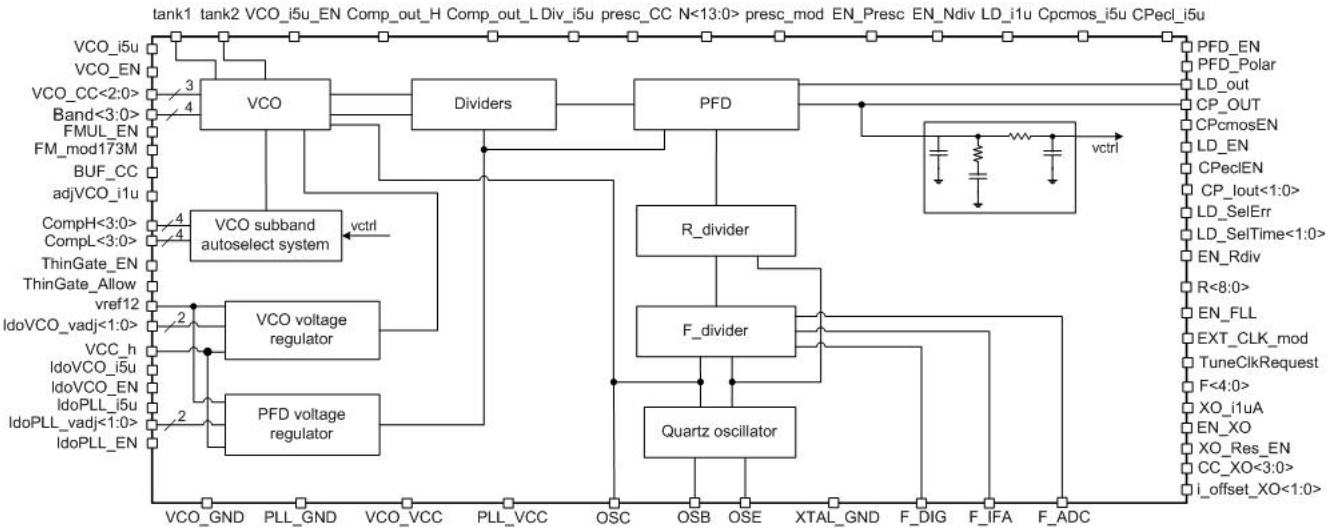

Figure 1: Phase-locked loop system structure

5 PIN DESCRIPTION

Name	Direction	Description
vref12	I	Voltage regulators reference voltage
XO_i1uA	IO	Reference oscillator reference current (1µA)
VCO_i5u	IO	VCO reference current (5µA)
Div_i5u	I	Dividers reference current (5µA)
LDi1u	I	Lock detector reference current (5µA)
CPcmos_i5u	I	CMOS charge pump reference current (5µA)
CPecl_i5u	I	ECL charge pump reference current (5µA)
ldoPLL_i5u	I	PLL voltage regulator reference current (5µA)
ldoVCO_EN	I	VCO voltage regulator enable/disable
adjVCO_i1u	IO	Comparator reference current controlling VCO voltage
LD_SelErr	I	Detection accuracy adjustment
LD_SelTime<1:0>	I	Detection period adjustment
LD_EN	I	Lock detector enable/disable
PFD_Polar	I	PFD polarity
CPcmos_EN	I	CMOS charge pump enable/disable
CP_Iout<1:0>	I	Charge pump output current control
CPeclEN	I	ECL charge pump enable/disable
PFD_EN	I	PFD enable/disable
Band<3:0>	I	Subband select
VCO_CC<2:0>	I	VCO core current consumption control
VCO_EN	I	VCO enable/disable
BUF_CC	I	Buffer current enable
FMUL_EN	I	Frequency multiplier enable/disable
FM_mod_173M	I	Frequency multiplier enable for frequency 140MHz
CC_XO<3:0>	I	Reference oscillator current control

Table “Pin Description” (continue).

Name	Direction	Description
i_offset_XO<1:0>	I	Reference oscillator offset current control
EN_XO	I	Reference oscillator enable/disable
XO_Res_EN	I	Reference current additional bias enable
N<13:0>	I	N-divider dividing ratio
R<8:0>	I	R-divider dividing ratio
Presc_mod	I	Prescaler type select
EN_Presc	I	Prescaler enable/disable
EN_Ndiv	I	N-divider enable/disable
EN_Rdiv	I	R-divider enable/disable
Presc_CC	I	Prescaler additional current enable
ThinGate_EN	I	Fixed bounds mode enable/disable
ThinGate_Allow	I	Voltage detector bounds type (VCO subband autoselect system)
CompH<3:0>	I	Voltage detector upper bound (VCO subband autoselect system)
CompL<3:0>	I	Voltage detector lower bound (VCO subband autoselect system)
TuneClkRequest	I	VCO subband autoselect system start
EN_FLL	I	Clock frequency divider enable/disable
Ext_Clk_mod	I	External reference frequency oscillator enable
F<4:0>	I	F-divider dividing ratio
ldo_PLL_vadj<1:0>	I	PLL output voltage control
ldo_VCO_vadj<1:0>	I	VCO output voltage control
ldoPLL_EN	I	PLL voltage regulator enable/disable
F_ADC	O	ADC clock frequency output
F_IFA	O	IFA clock frequency output
tank1	IO	VCO core outputs
tank2	IO	
CP_Out	IO	Charge pump current output
OSC	IO	Crystal oscillator analog output
OSB	IO	Analog output for crystal resonator connection
OSE	IO	Oscillator core collector output
Comp_out_H	O	VCO maximum required control voltage indicator
Comp_out_L	O	VCO minimum allowable control voltage indicator
VCO_i5u_EN	O	VCO voltage source reference current enable/disable (5 µA)
LD_out	O	Lock detector output
F_DIG	O	DSP clock frequency output
Xtal_GND	IO	Crystal oscillator ground
PLL_GND	IO	PLL ground
VCO_GND	IO	VCO ground
VCO_VCC	IO	VCO supply voltage
VCC_h	I	High level supply voltage
PLL_VCC	IO	PLL supply voltage

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions.

Dimension	Value	Unit
Height	941.49	µm
Width	2091.54	µm

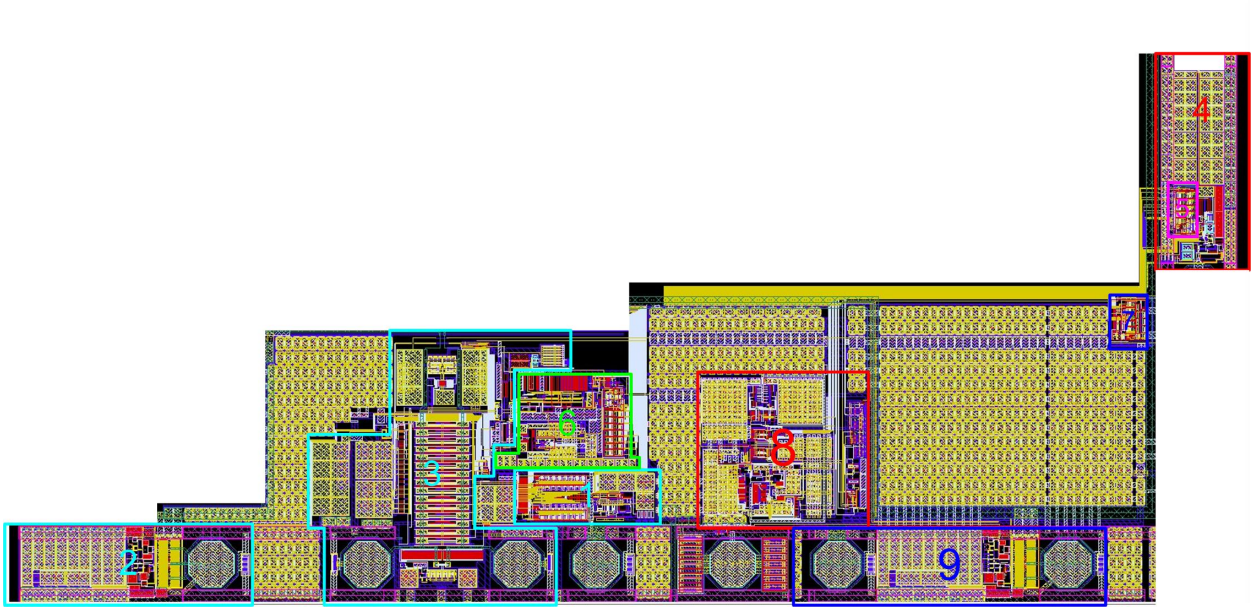

Figure 2: Device layout view

1. Voltage detector (VCO subband autoselect system)
2. VCO voltage regulator
3. VCO
4. Crystal oscillator
5. Crystal oscillator frequency divider
6. Dividers
7. Clock frequency dividers
8. PFD
9. PFD voltage regulator

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.78 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} =1.9 ÷ 2.3 V and T = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V and T = +27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	V_{cc}	-	1.9	2.2	2.3	V
Operating temperature range	T	-	-45	27	+85	°C
PLL division ratio	N_{PLL}	-	56	-	16383	-
Clock frequency	F_{clk}	For ADC	1.26	2.6	6.5	MHz
		For IFA	4.91	10.16	25.39	kHz
		For SPI	1.26	2.6	6.5	MHz
Reference frequency	F_{ref}	Depends on connected crystal; 1st harmonic of oscillator	-	26 57.647 78.325	-	MHz
Oscillation frequency range	F_{Osc}	At VCO operating	135	-	935	MHz
		At frequency multiplier operating	120	-	950	MHz
Peak-to-peak output voltage	A_{VCO}	-	300	-	-	mV
Peak –to-peak at clock frequency differential outputs	A_{cmos}	CMOS	1.9	2.2	2.3	V
R divider input frequency range	F_{IRO}	-	10	26	300	MHz
R divider programmable values	R_{PLL}	-	5	-	511	-
Comparison frequency range	F_{PFD}	-	-	0.1	1	MHz
Lock monitoring time	Sel_time	-	0.64	-	5.12	ms
Lock accuracy	Prec_lock	-	90	240	300	ns
Current consumption in an active mode	I_{cc}	-	0.94	1.11	1.54	mA
Current consumption in a standby mode	I_{stb}	-	-	8	120	nA
Oscillator phase noise spectral concentration	I_s	FPLL = 435 MHz FPFD = 100 kHz Tuning out 10 kHz	-	85	-	dBHz
Input logic-high level	V_{IH}	For digital inputs	0.7Vcc	-	Vcc+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

Table “Electrical Characteristics” (continue).

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Current consumption in a standby mode	I_{stb}	-	-	8	120	nA
Oscillator phase noise spectral concentration	I_s	F_{PLL} = 435 MHz F_{PFD} = 100 kHz Tuning out 10 kHz	-	85	-	dBHz
Input logic-high level	V_{IH}	For digital inputs	0.7V_{cc}	-	V_{cc}+0.25	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 3
- Subsection 7.2 update