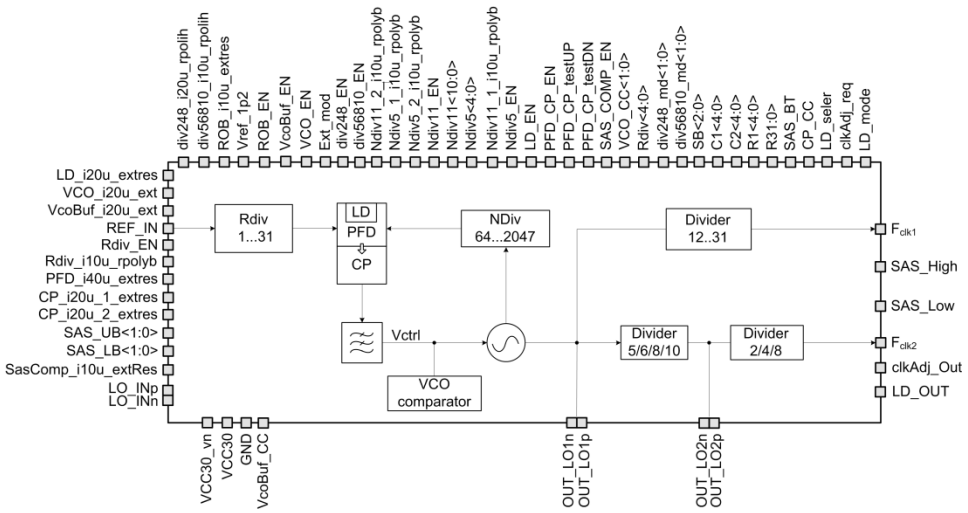
1.68 to 1.917 GHz Phase-Locked Loop

OVERVIEW

Frequency synthesizer built on PLL by dividing the integer coefficients. Synthesizer unit includes: R-divider of external reference oscillator frequency with a programmable division factor of 1 to 31, frequency-phase detector (PFD) with the charge pump, loop filter, a voltage controlled oscillator (VCO), VCO voltage control comparators, VCO frequency divider with programmable dividing ratio of 12 to 31, VCO frequency N-divider with programmable dividing ratio of 64 to 2047, 5/6/8/10 divider, 2/4/8 divider.



IP technology: AMS SiGe BiCMOS 0.350um.
IP status: silicon proven.
Area: 0.3mm^2

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.85	3.0	3.15	V
Operating temperature range	T_j	-	-60	27	+85	°C
1st oscillator frequency range	F_{LO1}	-	1692	1769	1973	MHz
2nd oscillator frequency range	F_{LO2}	-	175	-	225	MHz
1st oscillator peak-to-peak output voltage	A_{VCO}	Differential output	360	420	500	mV
PLL division ratio	N_{PLL}	-	64	-	2047	-
Reference frequency	F_{ref}	-	10	12.8	125	MHz
Reference frequency divider ratio	R_{PLL}	-	1	-	31	-
VCO phase noise at 1 MHz offset	PN_{VCO}	-	-	-	-119	dBc/Hz
Clock frequency	F_{CLK}	-	10	-	125	MHz
Clock frequency output voltage	A_{CLK}	Differential signal	460	-	700	mV
DC clock frequency output voltage	V_{DC_CLK}	Normal mode	-	V_{cc}-0.12	-	V
		LVDS mode	-	V_{cc}-1.75	-	V
Frequency synthesizer current consumption	I_{cc}	-	-	20.8	24.5	mA
Frequency synthesizer stand-by mode	I_{stby}	-	-	7	500	nA
Clock buffer current consumption in an active mode	I_{ccCLK}	-	1.6	1.8	2	mA
Clock buffer current consumption in stand-by mode	$I_{stbyCLK}$	-	-	3	100	nA
Input logic-level high	V_{IH}	For digital inputs	0.7V_{cc}	-	V_{cc}+0.3	V
Input logic-level low	V_{IL}		-	-	0.3V_{cc}	V